

Fermi National Accelerator Laboratory

PIXEL DETECTOR PROJECT

BTeV Pixel Detector Feed-Through Board Design Specifications

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Bradley Hall, Marcos Turquetti

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1 INTRODUCTION

This document describes the design specifications and functionality of the prototype BTeV Pixel Detector Feed-Through Board (FTB). The Pixel FTB is responsible for electrically connecting cabling from outside the pixel box to flex-circuits that reside inside the pixel box vacuum. These flex-circuits connected to pixel modules consisting of 4, 5, or 6 FPIX2 chips, the possibility of using a 8 FPIX2 module is also considered here.

Several constrains were taken in account during the design of the prototype, high magnetic fields prohibit the use of ferromagnetic components. The fact that half of the board is immerse in vacuum also contributed to constrains in the materials chosen to build the board. The temperature gradient also was observed during the design of this board

The Pixel FTB contains only passive components consisting of connectors and capacitors.

2 DESIGN FEATURES AND DEFINITIONS

This section describes the major features of the FTB design and the design assumptions used.

2.1 DESIGN ASSUMPTIONS

The design of the FTB is dependent on many mechanical and electrical constraints outline below:

- Pixel Station pitch is ~1.634" consisting of an "X" and a "Y" measuring plane
- X measuring plane contains 96 FPIX2 chips on 24 modules
- Y measuring plane contains 174 FPIX2 chips on 32 modules
- Module and flex-circuit pitch is .236" (6mm)
- All data and control signals are Low-Voltage Differential Signals (LVDS).

2.2 PIXEL MODULE CONSTRUCTION

Pixel modules consist of 4, 5 and 6 FPIX2 chips, it also consider the possibility of using a 8 FPIX2 chips module. The FPIX2 chips on each module share common control signals as well as a common digital and analog power. The FPIX2 chips on each pixel module are bump bonded to a single pixel sensor that requires a single high voltage bias channel. The X measuring plane contains 8x1 pixel sensors that span two 4-chip modules. These sensors can be biased from either of the two 4-chip modules. It's also possible that this 8x1 sensor being connected by a single 8-chip module.

2.2.1 COMMON CONTROL SIGNALS

Table 1 lists the clock and control signals that are common to all FPIX2 chips on a module.

2.2.2 COMMON CHARGE INJECT

Each module will have a single “charge-inject” signal that is connected to each FPIX2 chip. This signal is typically a saw-tooth voltage waveform from ~2V to ~1V and is terminated by a 50Ohm resistor on the module.

| <i>Clock/Control Signal</i> | <i>Description</i> |
|------------------------------------|---|
| MCLKA | 70MHz Clock |
| MCLKB | 70MHz Clock 90deg phased to MCLKA |
| BCOCLK | Bunch Crossing Clock (132ns, 7.57MHz) |
| SHIFTCTRL | Used for downloading configuration bit stream |
| SHIFTIN | Configuration bit stream data |
| SHIFTOUT | Configuration bit stream shift out |
| FFR | Fire Fighter Reset (hard reset) |
| OR | Operational Reset |

Table 1. Common module control signals.

2.2.3 POWER AND HIGH_VOLTAGE

Each module contains a single digital power (2.5V) and analog power (2.5V) channel that is used to power all FPIX2 chips on the module. A single high voltage bias (1000V DC max) is also provided for sensor biasing.

2.3 PIXEL PLANE CONSTRUCTION

Pixel planes are constructed from modules arranged on both the front and back sides of a substrate. A pixel plane consists of two halves (left and right side) that are brought together to create a complete plane. Figure 1 shows ½ of the Y Measuring plane. Both the left and right side of the Y Measuring plane are identical. Figure 2 shows the left side of the X Measuring plane. The right side of the X Measuring plane is identical to the left side with the exception that the corresponding modules are on the opposite side of the substrate.

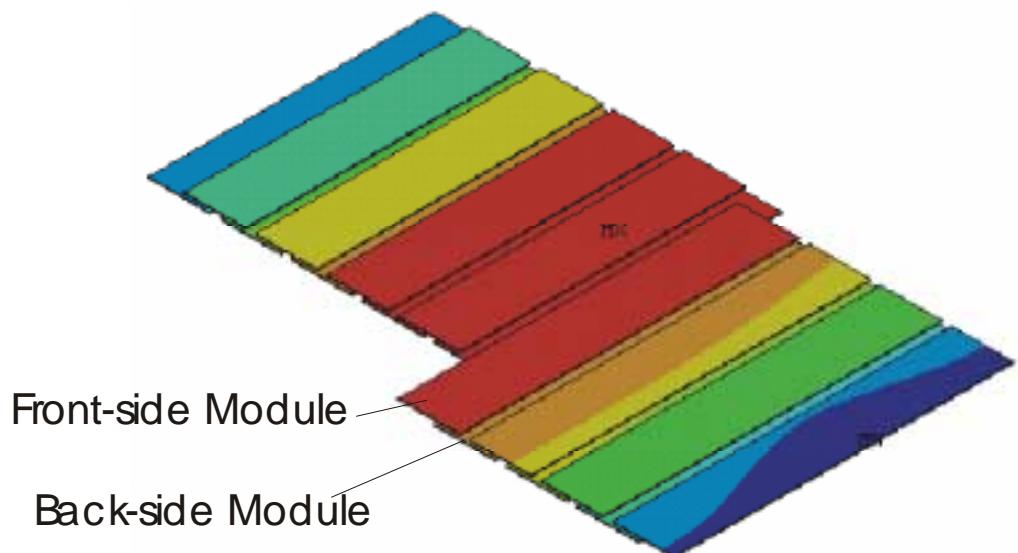


Image from C.M. Lei BTeVdoc-1560

Figure 1. $\frac{1}{2}$ of Y Measuring plane module arrangement (left and right).

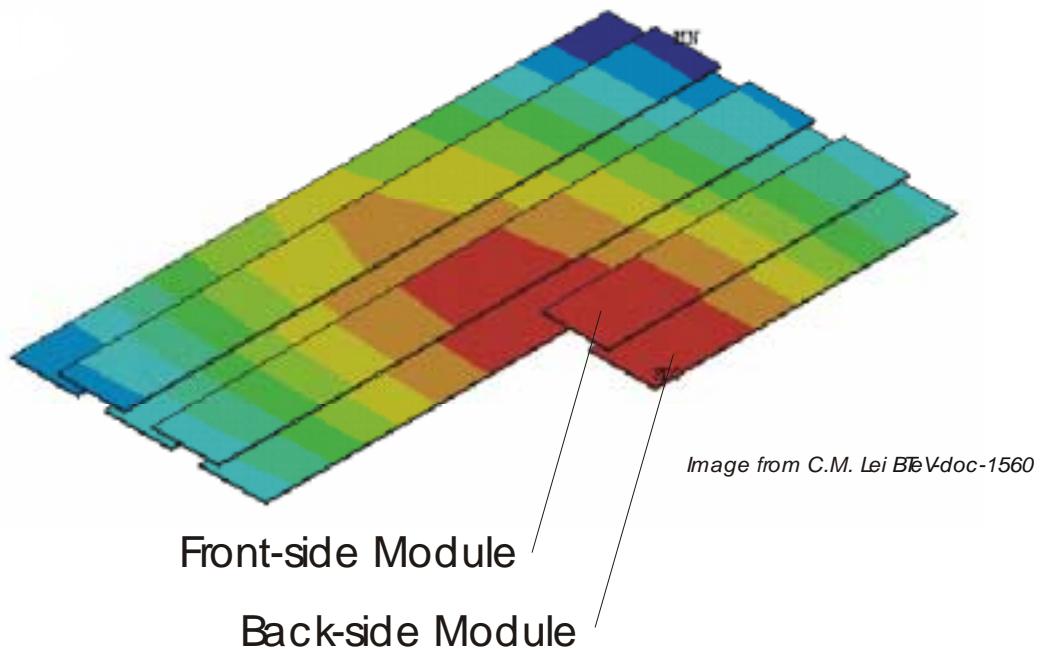


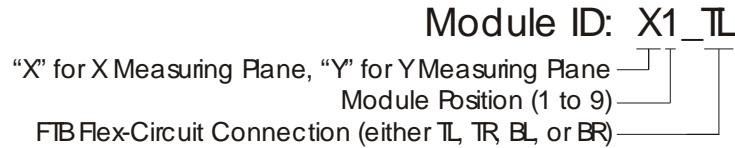
Image from C.M. Lei BTeVdoc-1560

Figure 2. $\frac{1}{2}$ of X Measuring plane module arrangement (left side).

2.4 PIXEL STATION AND MODULE IDENTIFICATION

This design assumes there are 30 pixel stations with each station consisting of an X Measuring plane and a Y Measuring plane.

Figure 3 and Figure 4 diagrams an entire pixel station showing both the X and Y measuring planes and identifies which modules are “front-side” modules and which modules are “back-side” modules. It also shows the serializer configuration each FPIX2 chip is assigned (1, 2, 4, or 6 serializers). Figure 3 and Figure 4 also assigns a module identification scheme using the following convention:



Module positions are numbered from the modules closest to the beam (starting at “1”) to those furthest from the beam. The “FTB Flex-Circuit Connection” refers to one of four possible FTBs the flex-circuit connecting that particular module is being routed to. These four possible FTBs are Top-Left (TL), Top-Right (TR), Bottom-Left (BL), and Bottom-Right (BR). The next section describes the flex-circuit routing in more detail.

| | | | | | | | | | | | | |
|--|---|---|---|---|---|---|---|---|---|---|---|--|
| Module ID: Y ₇ _TL Total Data & OutCLK 12 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Module ID: Y ₈ _TR Total Data & OutCLK 10 |
| Module ID: Y ₆ _TL Total Data & OutCLK 12 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Module ID: Y ₉ _TR Total Data & OutCLK 10 |
| Module ID: Y ₅ _TL Total Data & OutCLK 14 | 1 | 1 | 1 | 1 | 2 | 2 | 2 | 1 | 1 | 1 | 1 | Module ID: Y ₇ _TR Total Data & OutCLK 11 |
| Module ID: Y ₄ _TL Total Data & OutCLK 15 | 1 | 1 | 1 | 2 | 2 | 2 | 2 | 2 | 1 | 1 | 1 | Module ID: Y ₈ _TR Total Data & OutCLK 12 |
| Module ID: Y ₃ _TL Total Data & OutCLK 20 | 1 | 1 | 2 | 2 | 4 | 4 | 4 | 2 | 1 | 1 | 1 | Module ID: Y ₉ _TR Total Data & OutCLK 12 |
| Module ID: Y ₂ _TL Total Data & OutCLK 20 | 1 | 1 | 2 | 2 | 4 | 4 | 4 | 4 | 2 | 1 | 1 | Module ID: Y ₇ _TR Total Data & OutCLK 14 |
| Module ID: Y ₁ _TL Total Data & OutCLK 26 | 1 | 1 | 2 | 4 | 6 | 6 | 6 | 6 | 2 | 1 | 1 | Module ID: Y ₈ _TR Total Data & OutCLK 16 |
| Module ID: Y ₇ _BL Total Data & OutCLK 16 | 1 | 1 | 1 | 2 | 6 | | 0 | 2 | 1 | 1 | 1 | Module ID: Y ₉ _TR Total Data & OutCLK 16 |
| Module ID: Y ₂ _BL Total Data & OutCLK 16 | 1 | 1 | 1 | 2 | 6 | | 0 | 2 | 1 | 1 | 1 | Module ID: Y ₇ _TR Total Data & OutCLK 16 |
| Module ID: Y ₃ _BL Total Data & OutCLK 16 | 1 | 1 | 1 | 2 | 6 | | 0 | 0 | 4 | 2 | 1 | Module ID: Y ₈ _TR Total Data & OutCLK 26 |
| Module ID: Y ₄ _BL Total Data & OutCLK 14 | 1 | 1 | 1 | 2 | 4 | | 4 | 4 | 2 | 2 | 1 | Module ID: Y ₉ _TR Total Data & OutCLK 26 |
| Module ID: Y ₅ _BL Total Data & OutCLK 12 | 1 | 1 | 1 | 2 | 2 | | 4 | 4 | 2 | 2 | 1 | Module ID: Y ₇ _TR Total Data & OutCLK 20 |
| Module ID: Y ₆ _BL Total Data & OutCLK 12 | 1 | 1 | 1 | 2 | 2 | | 2 | 2 | 2 | 1 | 1 | Module ID: Y ₈ _TR Total Data & OutCLK 20 |
| Module ID: Y ₇ _BL Total Data & OutCLK 11 | 1 | 1 | 1 | 1 | 2 | | 2 | 2 | 1 | 1 | 1 | Module ID: Y ₉ _TR Total Data & OutCLK 15 |
| Module ID: Y ₈ _BL Total Data & OutCLK 10 | 1 | 1 | 1 | 1 | 1 | | 1 | 1 | 1 | 1 | 1 | Module ID: Y ₇ _TR Total Data & OutCLK 14 |
| Module ID: Y ₉ _BL Total Data & OutCLK 10 | 1 | 1 | 1 | 1 | 1 | | 1 | 1 | 1 | 1 | 1 | Module ID: Y ₈ _TR Total Data & OutCLK 12 |

Front-side Module
 Back-side Module

Figure 3. Y Measuring plane, numbers inside the yellow and green box indicate serializer configuration

It's possible to observe in Figure 3 that one Y plane is composed of 32 modules, 14 modules are (6x1) and 18 Modules are (5x1) a total of 174 FPIX2 readout chips and 32 detectors (one for each module).

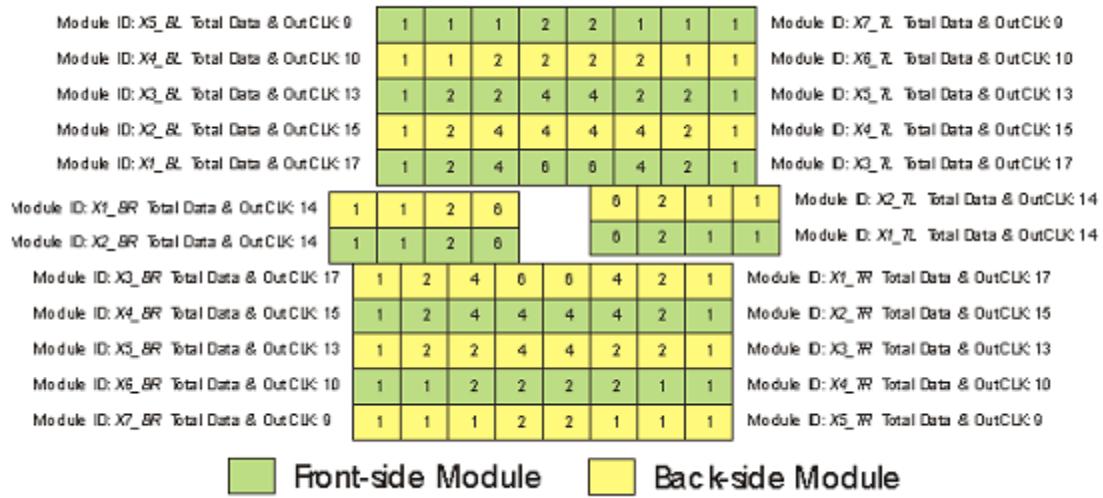


Figure 4. X Measuring plane. Pixel module identification scheme and serializer configuration.

In Figure 4 there are two possible different configurations. The first one with 24 modules all of them (4x1) and 14 detectors. The second possible configurations consist of 14 modules, 10 of them being (8x1) and 4 being (4x1), we have also a total of 14 detectors. In Figure 5 it's possible to observe the way the X and Y planes are put together forming the 30 stations.

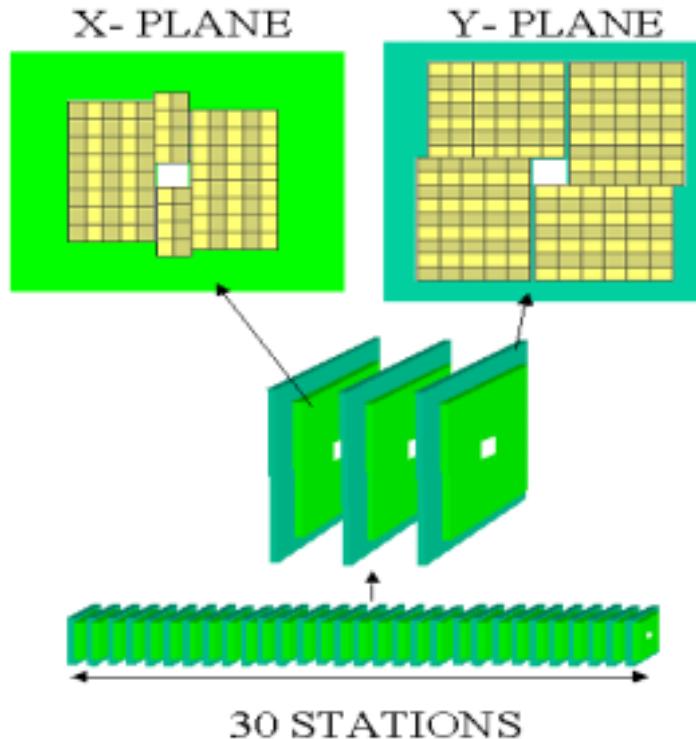


Figure 5. Assembly of X and Y planes.

2.5 FLEX-CIRCUIT ROUTING AND CONNECTIONS TO FTB

Figure 6 diagrams the beam-view of a single pixel station with flex-circuits being routed to four FTBs (TL, TR, BL, and BR). From this diagram it can be seen that each station routes $\frac{1}{4}$ of its modules to one FTB. Four FTBs are required to connect a complete pixel station. There are 56 modules in a pixel station, therefore each $\frac{1}{4}$ station is 14 modules. Figure 7 provides a 3-dimensional view of a few stations and their flex-circuit routing to the left side FTBs.

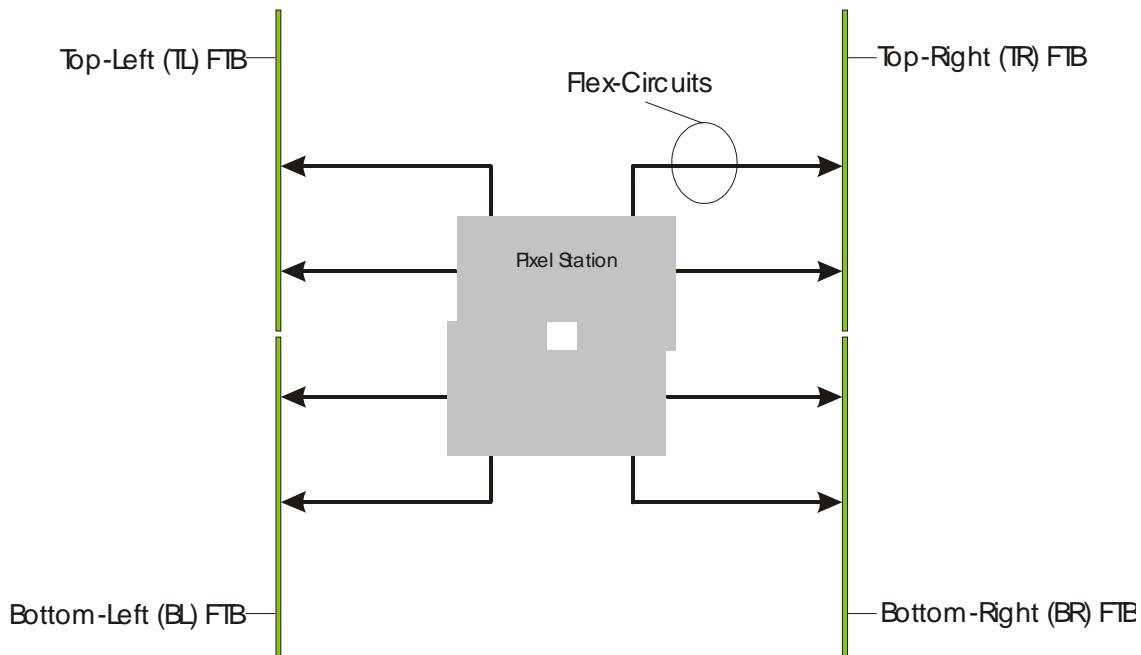


Figure 6. FTB locations (beam-view).

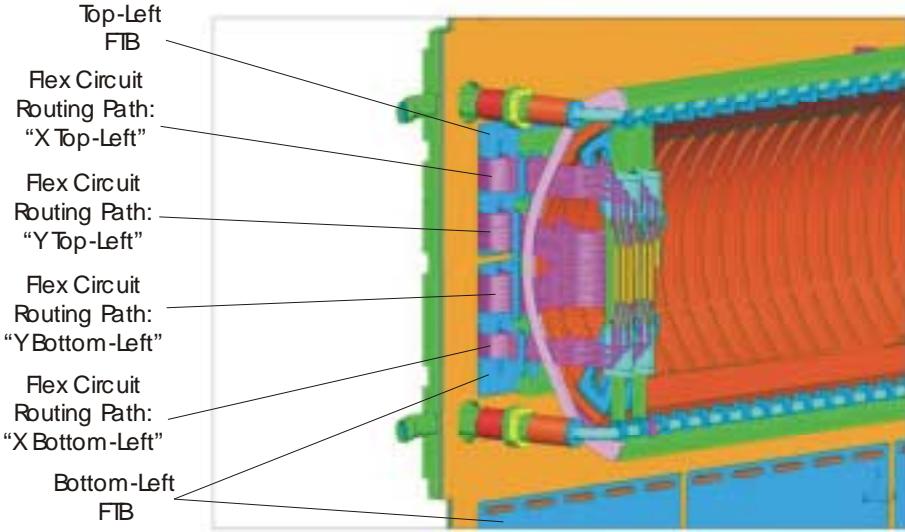


Figure 7. 3-D view of flex-circuit routing on left side (drawing by Alex Toukhtarov).

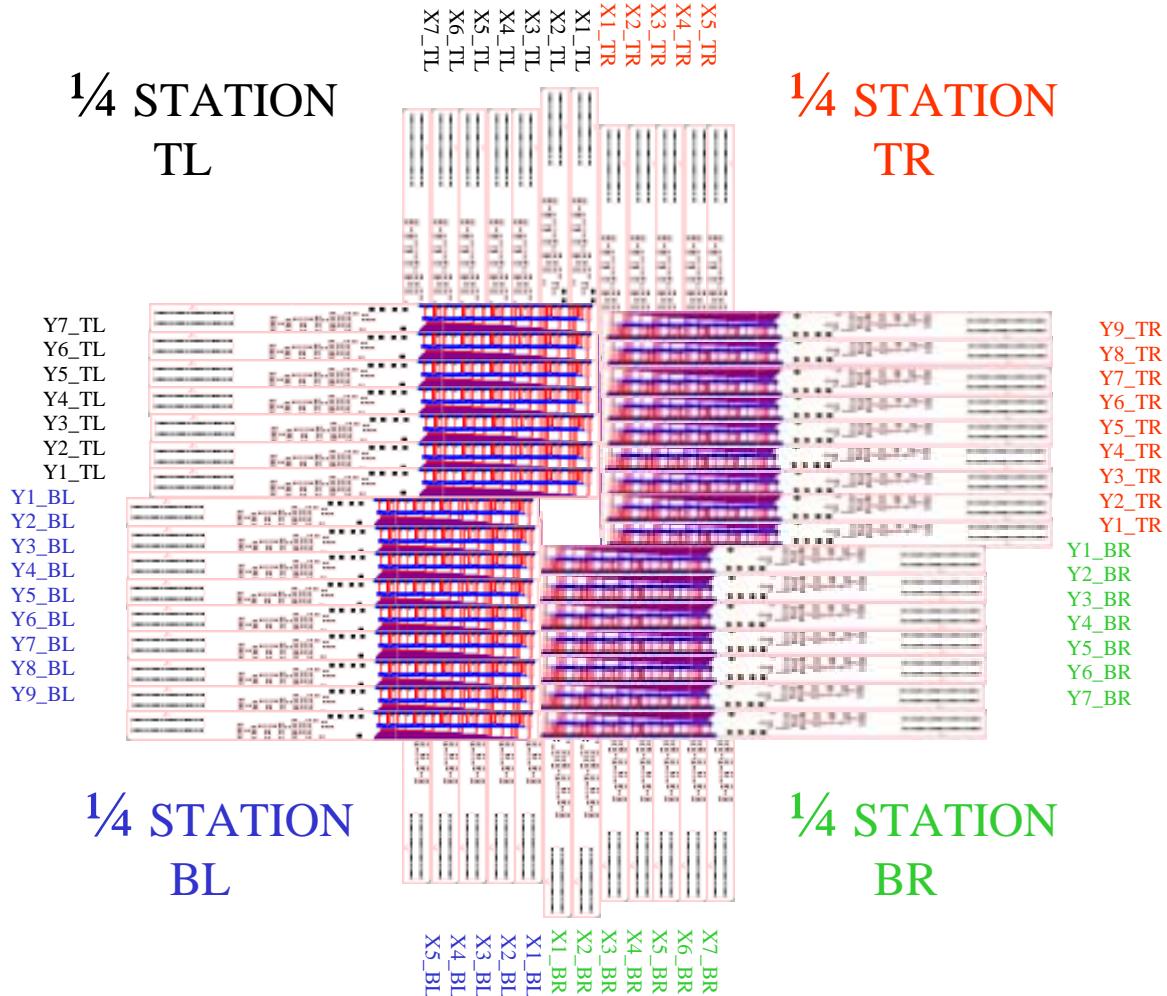


Figure 8. Routing patch from modules to FTB.

Figure 8 and Figure 9 shows the mapping wish the flex cables connecting the FTB to the modules should follow.

Each FTB is cable of connecting ten ¼ station, each station is connected to four different FTB, this arrangement can be better visualized Figure 6.

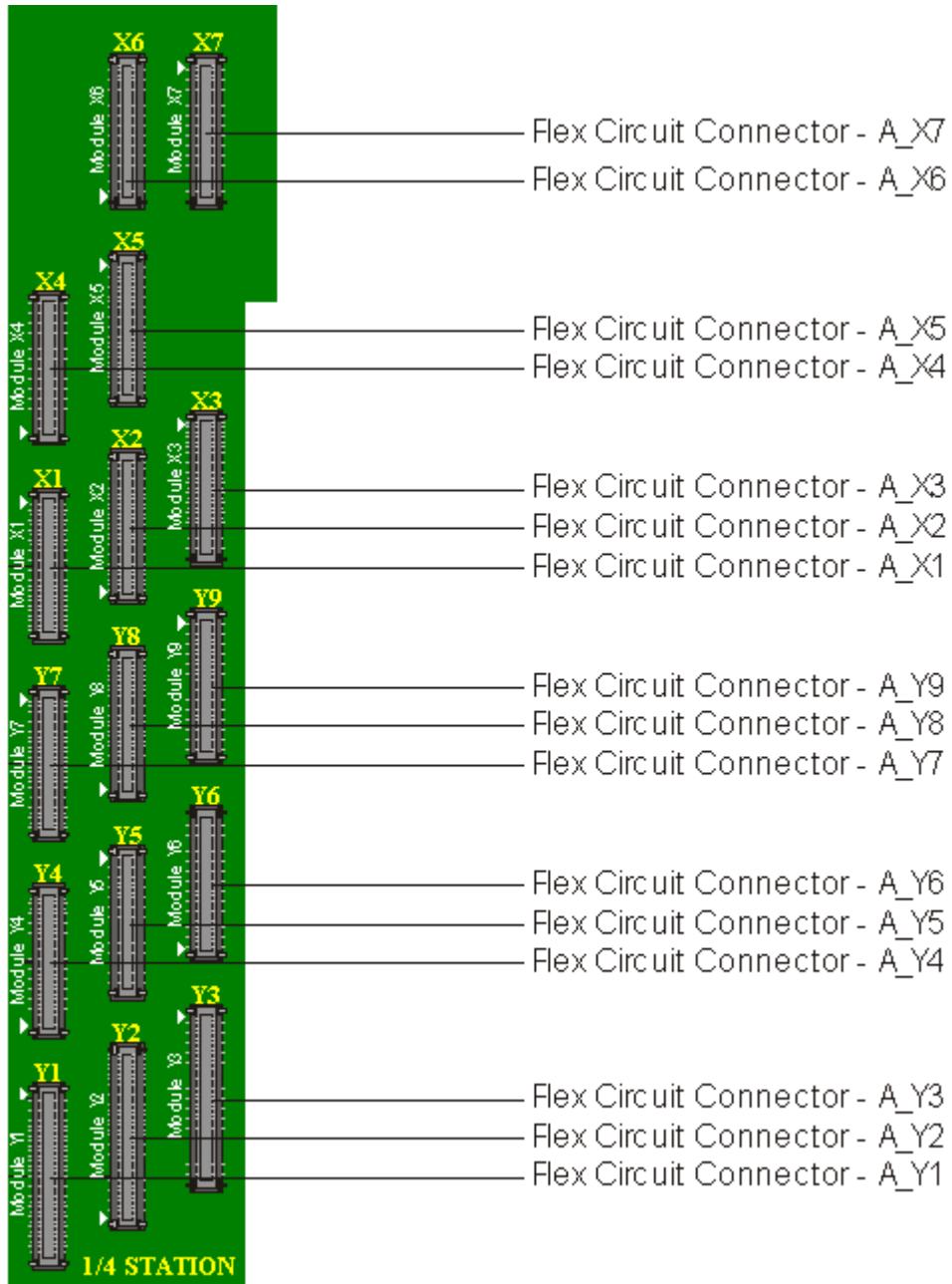


Figure 9. FTB connections with modules.

2.6 FTB KEY DIMENSIONS

Figure 10 diagrams some of the key FTB dimensions. The overall board dimensions are 27.5" x 17.0". There are ten mounting holes: five "top" mounting holes and five "middle" mounting holes. All of these holes shall be plated with an outer ring for good electrical connection to the aluminum plate it will be bolted to.

The red areas shown in Figure 10 indicates the areas of the board that will be machined (material removed) to form half-lap joints with adjacent boards. These edges shall be free from any electrical routing and components. The yellow areas shown in Figure 10 require that the surfaces (both top and bottom layer) be free of any electrical traces, components, and silk-screen. These surfaces will be bolted and glued to an aluminum support frame. The 2.25" wide yellow band in the middle will accommodate the vacuum feed-through. Components above this 2.25" band are outside the vacuum while those below are inside the vacuum.

The white slots on the bottom of the diagram shown in Figure 10 are 0.2" x 6.0" openings that allow the pixel module flex cables to pass through and make connections to the back side of the FTB.

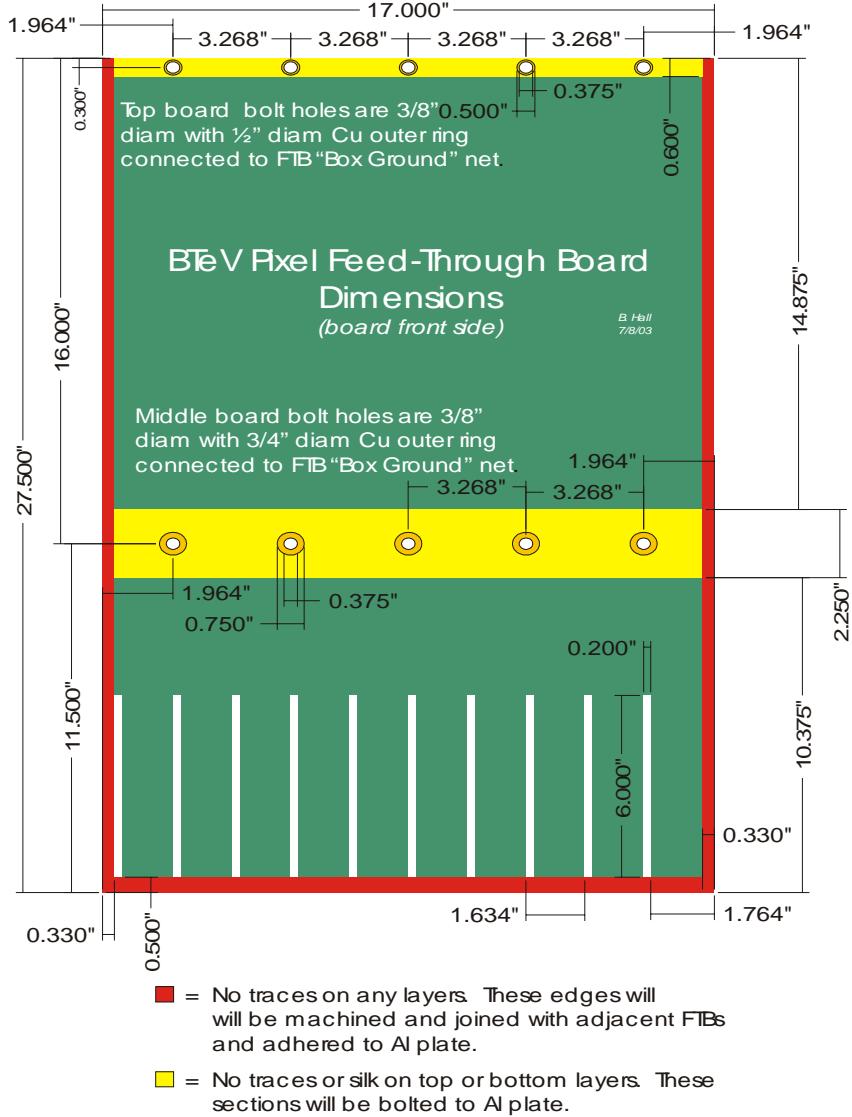


Figure 10. FTB key dimensions.

Complete View of FTB and FTBs in Assembly Plate Figure 11 and Figure 12 show the complete front and back side FTB, respectively. The details of the components will be described in the next section. Each FTB will connect ten pixel $\frac{1}{4}$ stations (labeled A through J). Components populate both on the front and the back side of the board outside the vacuum and on the back side only inside the vacuum. Slots on the board inside the vacuum allow for passage of flex-circuits connecting pixel modules.

Figure 13 shows the FTB assembly plate with six FTBs installed. The FTB assembly plate is part of the mechanical assembly of the pixel-detector box. It provides a structural frame for the FTBs as well as impose mechanical constraints impacting the FTB design. There will be two FTB assembly plates for the pixel detector system – one for the left side and one for the right side. Each FTB assembly plate will accommodate six FTBs (three top and three bottom) for a total of twelve FTBs for the entire pixel detector system.

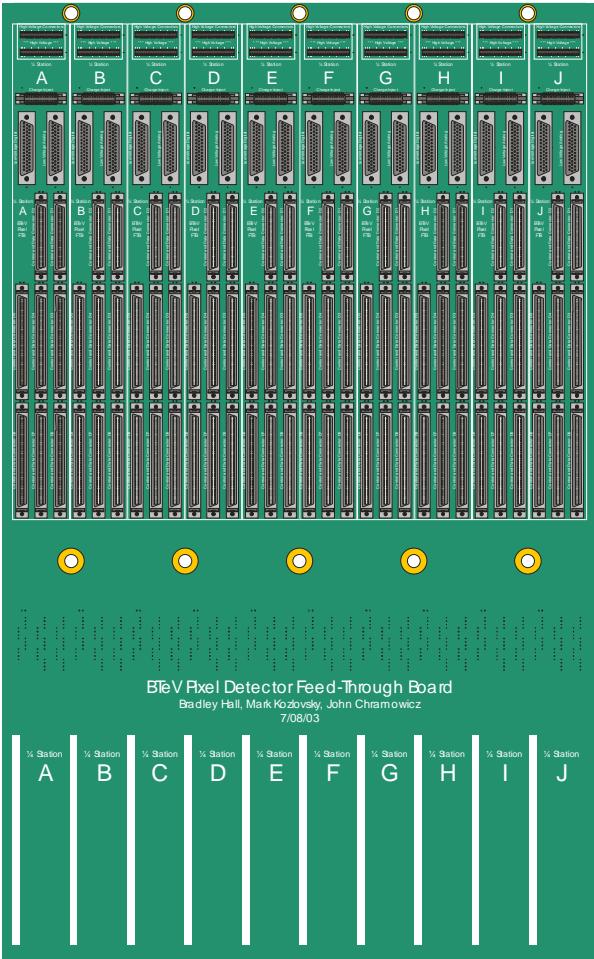


Figure 11. Front side view of FTB

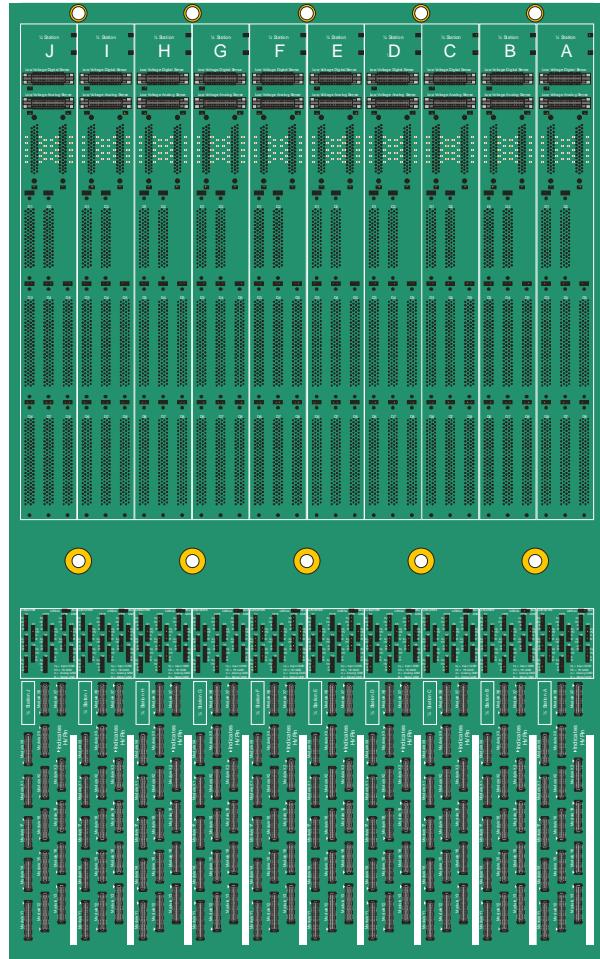


Figure 12. Back side view of FTB.

In Figure 13 it's possible to observe six of the twelve FTB boards that will compose the system, as it can be visualized in Figure 6 the other six board are facing the boards showed in that figure.

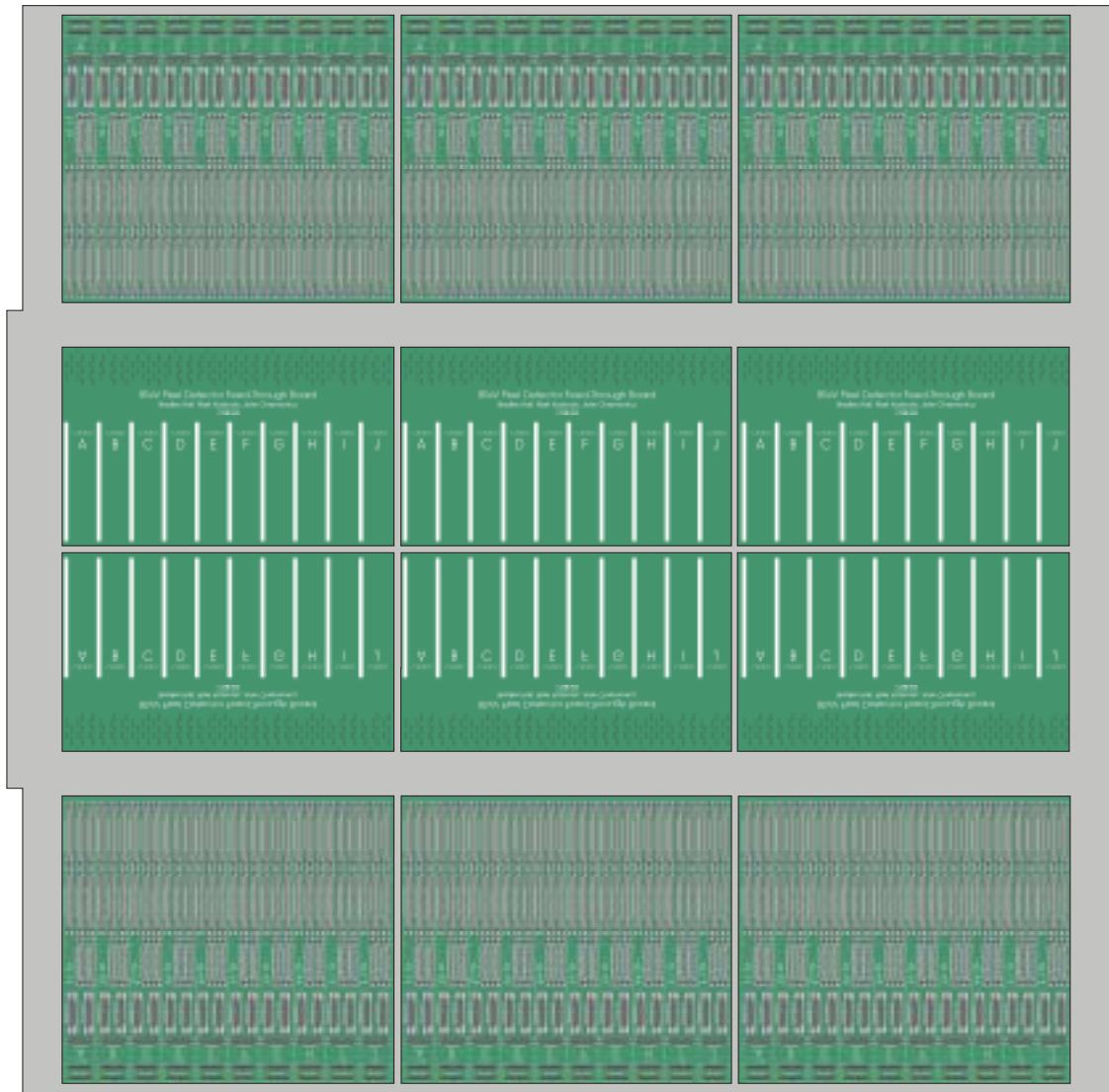


Figure 13. Assembly plate with FTBs installed.

3 COMPONENTS AND COMPONENT PLACEMENT

This section describes the components required to build the FTB and their suggested location on the board.

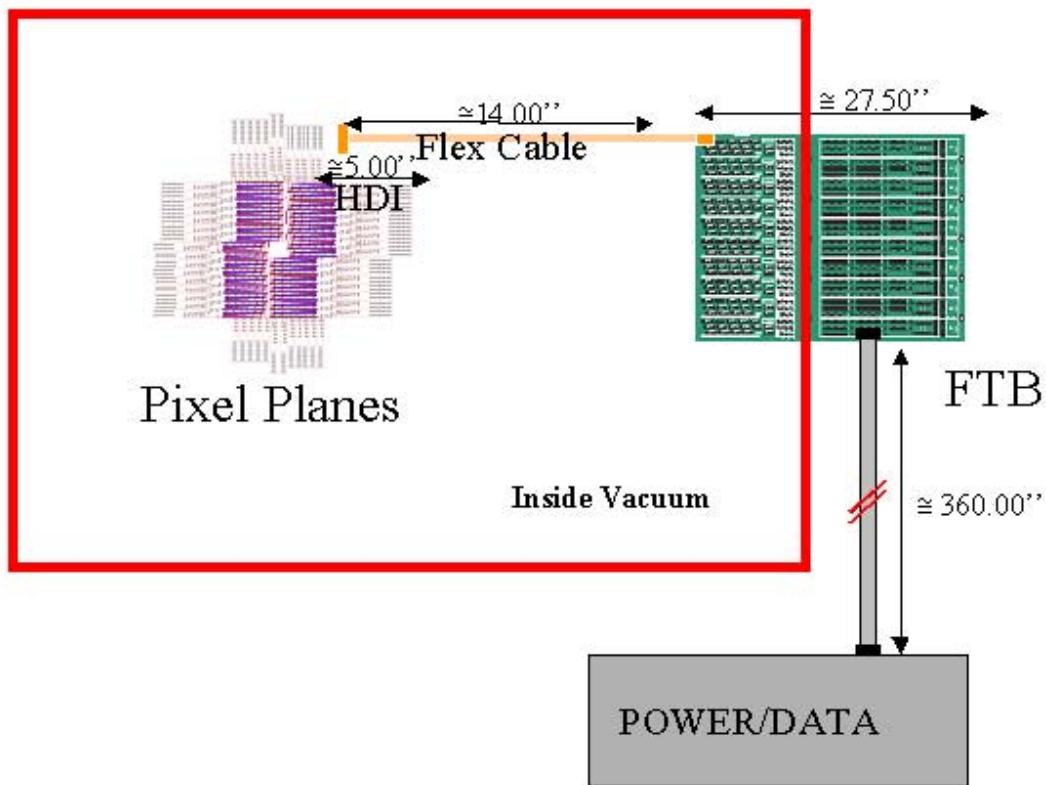


Figure 14. Schematic showing components inside the vacuum and outside

3.1 OUTSIDE VACUUM COMPONENTS AND PLACEMENT

Tables 2 through 8 describe all of the required components that reside outside the vacuum. Figure 15 diagrams a $\frac{1}{4}$ station section of the FTB showing all of the outside components and their suggested location. This figure shows connector required for only one of the ten $\frac{1}{4}$ stations each FTB is designed to accommodate. The connectors and layout for $\frac{1}{4}$ stations A should be the same for $\frac{1}{4}$ stations B, C, D, E, F, G, H, I, and J.

3.1.1 DATA AND CONTROL

| | Pins used | Connector size (pins) | Cable number of conductors |
|----|-----------|-----------------------|----------------------------|
| D1 | 68 | 68 | 68 |
| D2 | 68 | 68 | 68 |
| D3 | 96 | 100 | 100 |
| D4 | 96 | 100 | 100 |
| D5 | 100 | 100 | 100 |
| D6 | 96 | 100 | 100 |
| D7 | 96 | 100 | 100 |
| D8 | 96 | 100 | 100 |

8 Cables per 1/4 station
 80 Cables per FTB
Total=960 Cables for all system

Two types of cables:

3M #90201/100
 3M #90201/68

| | |
|---|--|
|  | <i>Manufacturer:</i> 3M <i>Part #:</i> 82068-600X <i>Qty per FTB:</i> 20 |
| 68 pin MDR connector for LVDS data and control signals. | |

Table 5. 68-pin data and control signals connector.

| | |
|---|--|
|  | <i>Manufacturer:</i> 3M <i>Part #:</i> 82100-600X <i>Qty per FTB:</i> 60 |
| 100 pin MDR connector for LVDS data and control signals. | |

Table 6. 100-pin data and control signals connector.

3.1.2 LOW VOLTAGE POWER

| | Pins used | Connector size (pins) | Cable number of conductors |
|---------|-----------|-----------------------|----------------------------|
| Analog | 28 | 44 | 32 |
| Digital | 28 | 44 | 32 |

2 Cables per 1/4 station

20 Cables per FTB

Total=240 Cables for all system

One type of cable:
Alpha Wire #5610B2016 (12 pairs)

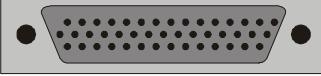
| | |
|---|--|
|  | <i>Manufacturer:</i> NorComp <i>Part #:</i> 180-044-212-001 <i>Qty per FTB:</i> 20 |
| 44 Pin D-Sub connector for both Digital and Analog low voltage power. | |

Table 2. Digital and Analog power connector.

3.1.3 SENSE WIRE

| | Pins used | Connector size (pins) | Cable number of conductors |
|---------------------|-----------|-----------------------|----------------------------|
| Sense Wire(Analog) | 29 | 36 | 36 |
| Sense Wire(Digital) | 29 | 36 | 36 |

2 Cables per 1/4 station

20 Cables per FTB

Total=240 Cables for all system

One type of cable:
3M #90201/036 (.025" Pleated Foil Shielded)

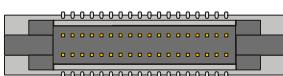
| | |
|--|--|
|  | <i>Manufacturer:</i> 3M <i>Part #:</i> 81036-660C00 <i>Qty per FTB:</i> 30 |
| 36 pin .05" pitch connector used for Low-Voltage Digital sense, Low-Voltage Analog sense, and Charge-Inject. | |

Table 3. Voltage sense and charge-inject connector.

3.1.4 CHARGE INJECTION

| | Pins used | Connector size (pins) | Cable number of conductors |
|------------------|-----------|-----------------------|----------------------------|
| Charge Injection | 29 | 36 | 36 |

1 Cable per ¼ station
 10 Cables per FTB
Total=120 Cables for all system

One type of cable:
 3M #90201/36

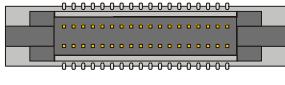
| | |
|--|--|
|  | <i>Manufacturer:</i> 3M <i>Part #:</i> 81036-660C00 <i>Qty per FTB:</i> 30 |
| 36 pin .05" pitch connector used for Low-Voltage Digital sense, Low-Voltage Analog sense, and Charge-Inject. | |

Table 3. Voltage sense and charge-inject connector.

3.1.5 HIGH VOLTAGE

| | Pins used | Connector size (pins) | Cable number of conductors |
|-----|-----------|-----------------------|----------------------------|
| HV1 | 15 | 48 | 2 |
| HV2 | 15 | 48 | 2 |

* 2 pins are shield

14 Cables per ¼ station
 140 Cables per FTB
Total=1380 Cables for all system

One type of cable:
 Coax 50Ohm RG58C/U (1600V max)

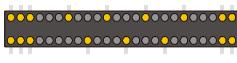
| | |
|--|---|
|  | <i>Manufacturer:</i> Omnetics <i>Part #:</i> TBD <i>Qty per FTB:</i> 20 |
| Custom high voltage connector from Omnetics, Inc. 1000V DC. Seven high voltage channels per connector. | |

Table 4. High-voltage connector.

| |
|--|
|  <i>Manufacturer:</i> Molex <i>Part #:</i> 22-28-4023 <i>Qty per FTB:</i> 80 |
| Jumper for connecting data and control cable shield to box ground. |

Table 7. 2-pin straight header.

| |
|--|
|  <i>Manufacturer:</i> Molex <i>Part #:</i> 22-28-4023 <i>Qty per FTB:</i> 70 |
| Post for cable shield connection. This is one-half of part# 22-28-4023. |

Table 8. 1-pin post.

| |
|--|
|  <i>Manufacturer:</i> Panasonic <i>Part #:</i> ECJ-2FB0J475M <i>Qty per FTB:</i> 280 |
| 0805 4.7 μ F capacitor for decoupling Vddd and Vdda power. |

Table 9. 4.7 μ F decoupling capacitor.

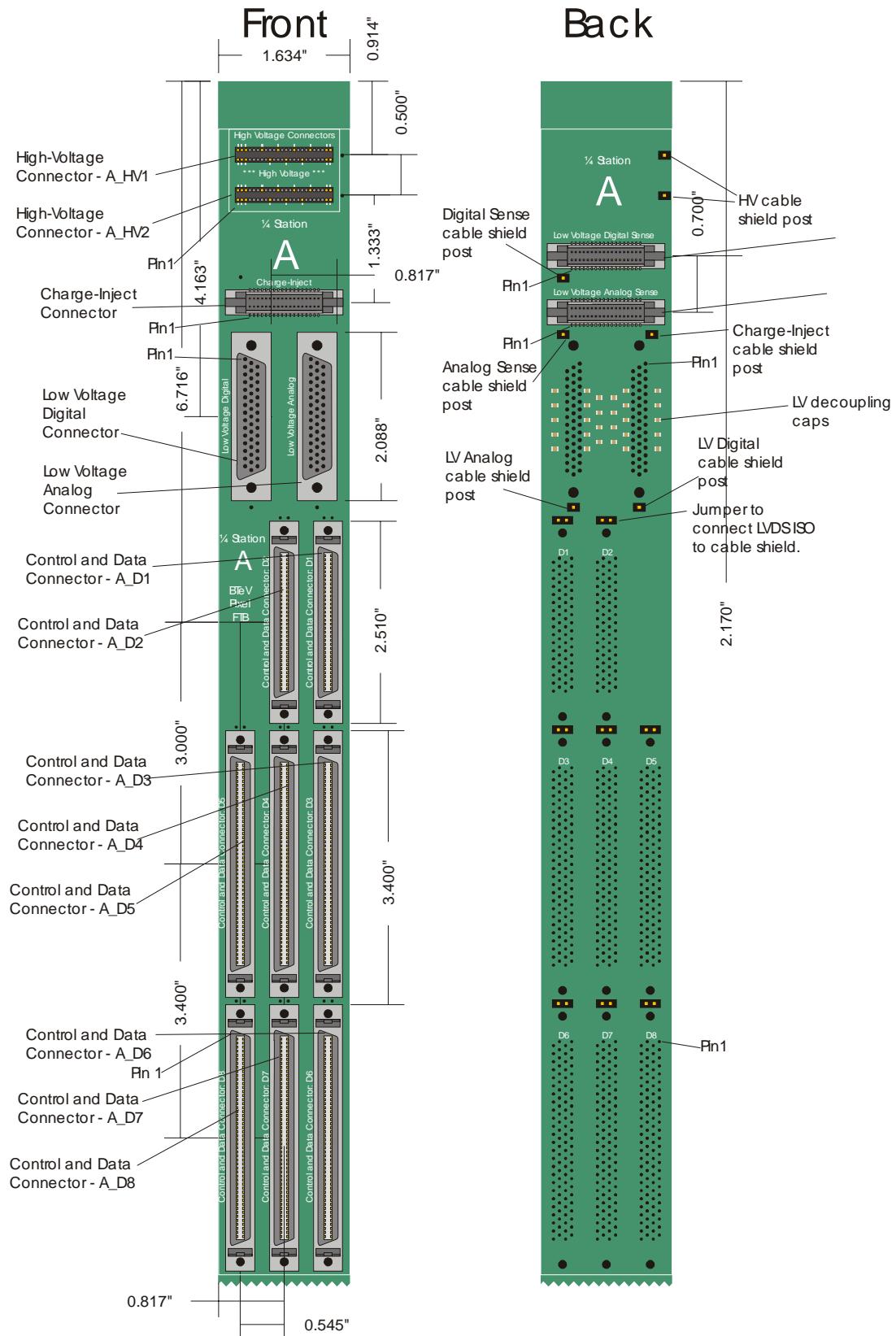


Figure 15. Outside vacuum components placement for one 1/4 station.

3.2 INSIDE VACUUM COMPONENTS AND PLACEMENT

Tables 10 to 15 describe the components used inside the vacuum for connecting module flex-circuits and for configuring ground returns. Figure 16 diagrams the component placement for one ¼ station. Note that this figure shows one ¼ station A, however, ¼ station B, C, D, E, F, G, H, I, and J are identical.

Figure 16 diagrams the modified flex-circuit connectors. Each flex-circuit connector connects one pixel module. The flex-circuit connector contains high voltage, low voltage, low voltage sense, as well as data and control. There are four types of flex-circuit connectors: a stock 100-pin connector with a solder tab and pins 2-7 removed, a stock 100-pin connector with a solder tab and pins 44-49 removed, a stock 80-pin connector with a solder tab and pins 2-7 removed, and a stock 80-pin connector with a solder tab and pins 34-39 removed.

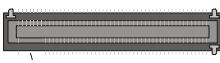
| | |
|---|---|
|  | <i>Manufacturer:</i> Molex <i>Part #:</i> 54363-1008 <i>Qty per FTB:</i> 20 |
| Modified 100-pin flex-circuit connector with pins 2-7 removed and a solder tab removed. | |

Table 10. Modified 100-pin flex-circuit connector.

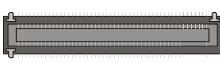
| | |
|---|---|
|  | <i>Manufacturer:</i> Molex <i>Part #:</i> 54363-1008 <i>Qty per FTB:</i> 10 |
| Modified 100-pin flex-circuit connector with pins 44-49 removed and a solder tab removed. | |

Table 11. Modified 100-pin flex-circuit connector.

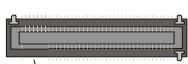
| | |
|--|---|
|  | <i>Manufacturer:</i> Molex <i>Part #:</i> 54363-0808 <i>Qty per FTB:</i> 70 |
| Modified 80-pin flex-circuit connector with pins 1-7 removed and a solder tab removed. | |

Table 12. Modified 80-pin flex-circuit connector.

| | |
|--|---|
|  | <i>Manufacturer:</i> Molex <i>Part #:</i> 54363-0808 <i>Qty per FTB:</i> 60 |
| Modified 80-pin flex-circuit connector with pins 34-39 removed and a solder tab removed. | |

Table 13. 80-pin flex-circuit connector.

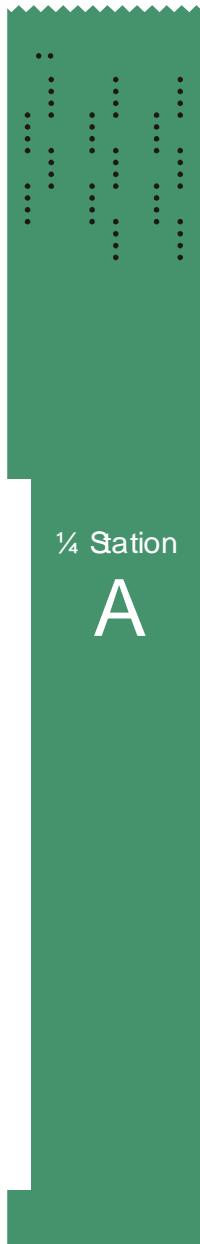
| | |
|---|--|
|  | <i>Manufacturer:</i> Molex <i>Part #:</i> 22-28-4043 <i>Qty per FTB:</i> 140 |
| 4-pin post used in ground configuration area. | |

Table 14. 4-pin straight header.

| | |
|---|--|
|  | <i>Manufacturer:</i> Molex <i>Part #:</i> 22-28-4023 <i>Qty per FTB:</i> 10 <i>Data Sheet:</i> 2-pin post used in ground configuration area. |
|---|--|

Table 15. 1-pin straight header.

Front



Back

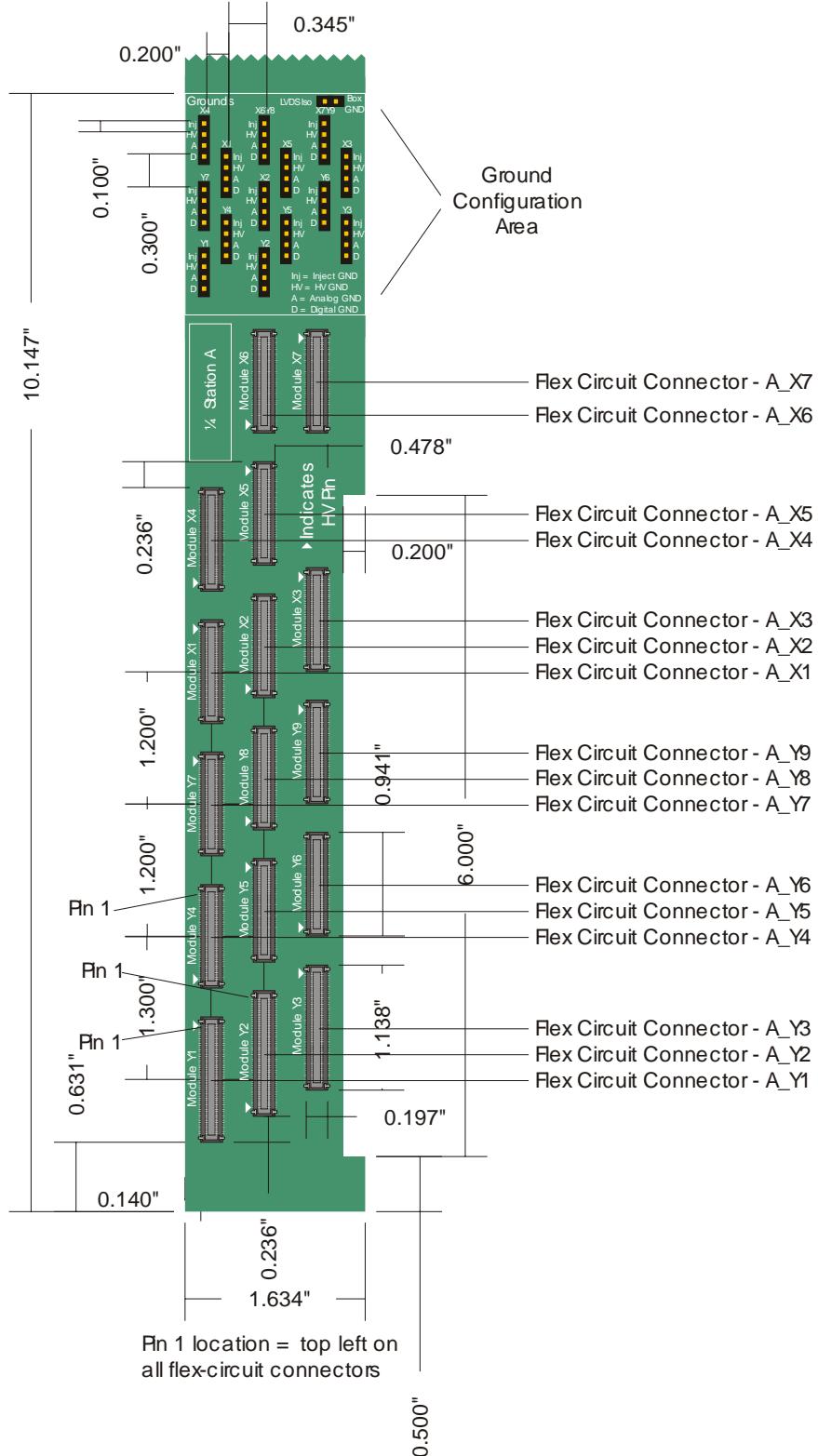


Figure 16. Inside vacuum components placement for one $\frac{1}{4}$ station.

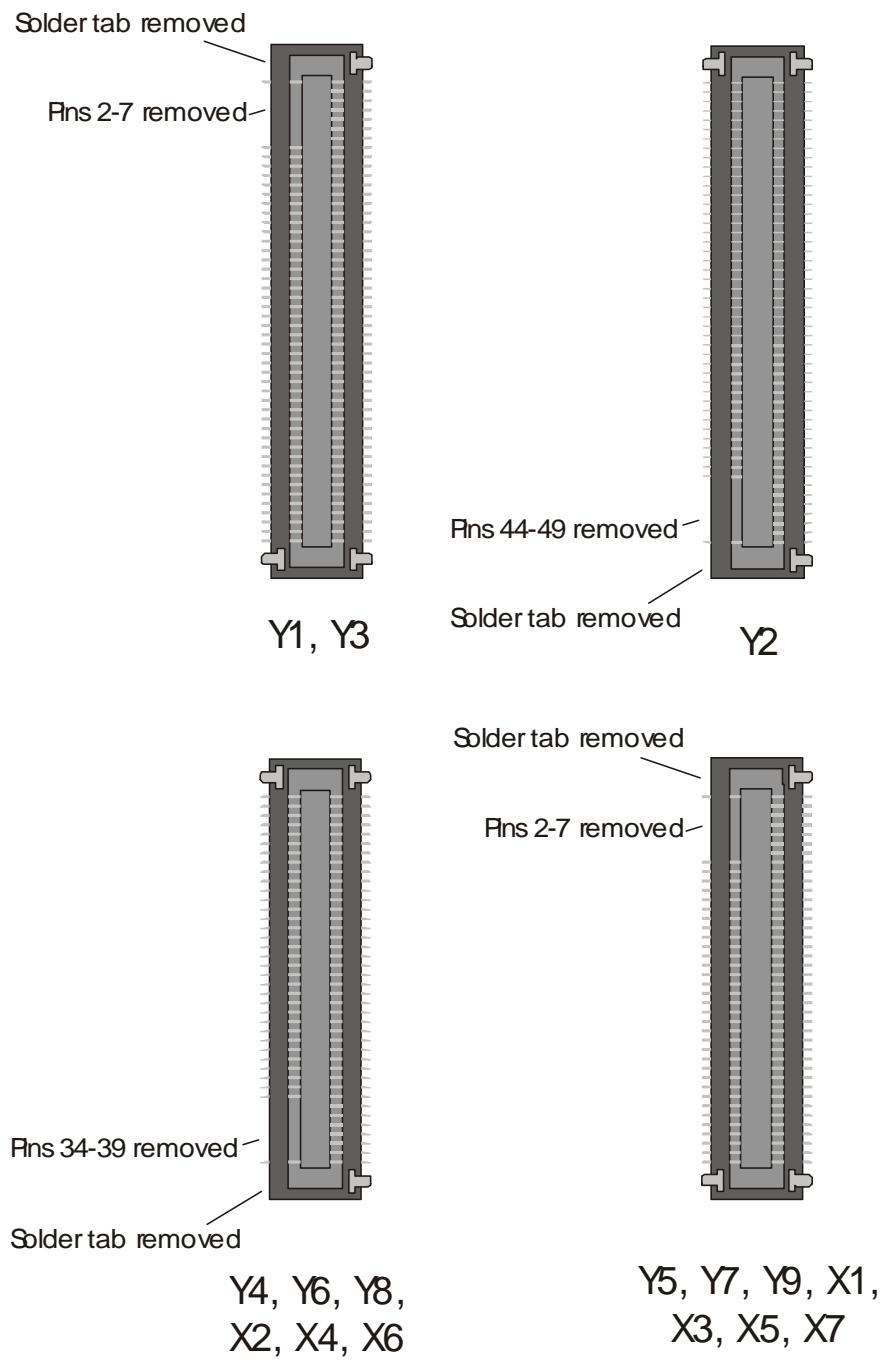


Figure 17. Modified flex-circuit connectors.

4 SIGNAL MAPPING

This section describes the signal mapping between the connectors outside the vacuum and those inside the vacuum. Note that this section describes the signal assignments for pixel ¼ stations A, however, the signal assignment for ¼ stations B, C, D, E, F, G, H, I, and J are identical to A after replacing the net name prefix with the appropriate ¼ station letter identifier.

Note that at the creation time of this document, the FPIX2 pixel module and flex-circuit have not been designed and therefore have not imposed a pin assignment constraint on the FTB flex-circuit connector. It is not the intention of the FTB design to impose a pin assignment constraint on the flex circuit and/or pixel module, therefore, the data and control signal names are general purpose I/O names.

Flex-circuits X6 and Y8 as well as X7 and Y9 share signals. This is done because there is no situation where these module pairs would be connected together on the same FTB at the same time.

4.1 GROUNDS

The FTB has no common Ground plane, instead there are the six types of ground/ground return signals described in Table 16. The trace widths for the return signals (HV Return, LV Digital Return, LV Analog Return, and Charge-Inject Return) should be the same trace width as their corresponding supply signal.

Figure 18 diagrams the ground configuration area on the back side of the FTB just above the flex circuit connectors. Straight post headers shall be used to provide access to all of the ground and ground return signals for flexibility in experimenting with ground connections.

| <u>Ground/Return</u> | <u>Quantity</u> |
|-----------------------|--|
| LVDS Isolation Ground | One per FTB |
| Box Ground | One per FTB |
| HV Return | One per HV channel (14 per ¼ station) |
| LV Digital Return | One per LV Digital channel (14 per ¼ station) |
| LV Analog Return | One per LV Analog channel (14 per ¼ station) |
| Charge-Inject Return | One per charge-inject channel (14 per ¼ station) |

Table 16. Grounds and Ground Returns.

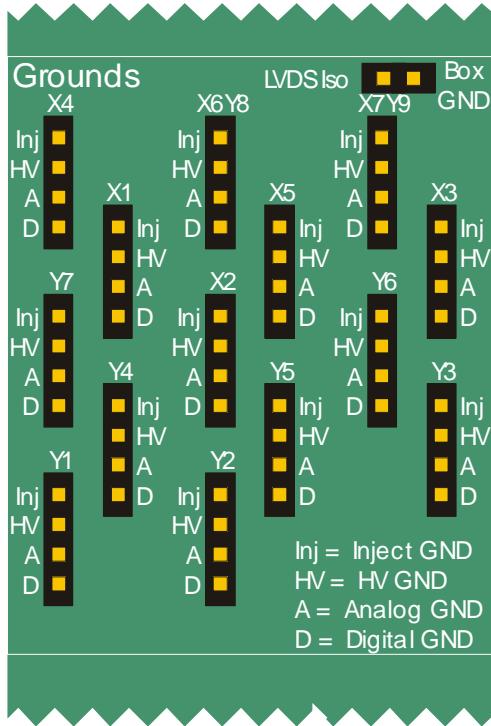


Figure 18. Ground configuration area for one 1/4 station.

4.2 CABLE SHIELDING

All of the outside vacuum cabling that connects to the FTB will be shielded. The shields from these cables will be either electrically connected to the treaded mounting holes (low voltage and data/control connectors) or to pin 1 (all other connectors). Table 17 summarizes the seven outside vacuum connector types and their cable shield connection point.

All cable shield connections should be made available on a 1 or 2-pin post adjacent to the connector and on the back side of the board (as shown in Figure 15). The 2-pin post adjacent to the data and control cables should contain the data and control cable shield on one pin and the LVDS Isolation connection on the other.

| <u>Connector</u> | <u>Cable Shield Connection From</u> |
|------------------|-------------------------------------|
| Data and Control | Mounting screws |
| LV Digital | Mounting screws |
| LV Analog | Mounting screws |
| LV Digital Sense | Connector pin 1 |
| LV Analog Sense | Connector pin 1 |
| Charge-Inject | Connector pin 1 |
| High Voltage | Connector pin 1 |

Table 17. Connectors and cable shield connection point.

4.3 IMPEDANCE CONTROL

It is critical that all data and control signal trace pairs be impedance controlled to 100Ω . All signaling is Low Voltage Differential Signal (LVDS) and will be connected to $\sim 10\text{m}$ of cabling outside the vacuum. The LVDS standard requires 3.5mA of current with a 100Ohm termination. Maximum switching frequency for the FTB application will be 70MHz. Figure 19 offers a suggested layout technique for routing LVDS pairs. Note that there must be an LVDS Isolation plane between pair layers.

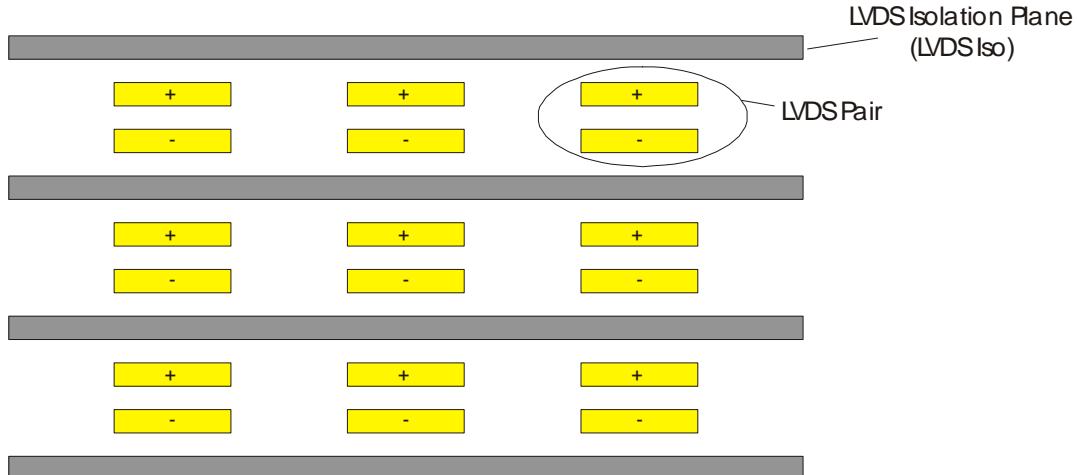


Figure 19. Suggested LVDS pair routing with LVDS isolation plane.

4.4 DIGITAL POWER CONNECTOR

The Digital Voltage connector provides digital power to the FPIX2 modules. Each connector provides digital power to one $\frac{1}{4}$ station. The operating voltage for each V_{ddd} channel is 2.5V with 800mA maximum current. Trace widths should be wide enough to accommodate a less than 10% voltage drop over the length of trace. For $\frac{1}{2}$ oz copper, the suggested trace width is 130 mil. Table 18 offers a suggested pin assignment.

| <i>Digital Power Connector</i> | | | |
|--------------------------------|---------------|--------------|---------------|
| <i>Pin #</i> | <i>Signal</i> | <i>Pin #</i> | <i>Signal</i> |
| 1 | No Connect | 2 | No Connect |
| 3 | No Connect | 4 | No Connect |
| 5 | No Connect | 6 | No Connect |
| 7 | No Connect | 8 | No Connect |
| 9 | A_X1_Vddd | 10 | A_X1_DGND |
| 11 | A_X2_Vddd | 12 | A_X2_DGND |
| 13 | A_X3_Vddd | 14 | A_X3_DGND |
| 15 | A_X4_Vddd | 16 | A_X4_DGND |
| 17 | A_X5_Vddd | 18 | A_X5_DGND |
| 19 | A_X6Y8_Vddd | 20 | A_X6Y8_DGND |
| 21 | A_X7Y9_Vddd | 22 | A_X7Y9_DGND |
| 23 | A_Y1_Vddd | 24 | A_Y1_DGND |
| 25 | A_Y2_Vddd | 26 | A_Y2_DGND |
| 27 | A_Y3_Vddd | 28 | A_Y3_DGND |
| 29 | A_Y4_Vddd | 30 | A_Y4_DGND |
| 31 | A_Y5_Vddd | 32 | A_Y5_DGND |
| 33 | A_Y6_Vddd | 34 | A_Y6_DGND |
| 35 | A_Y7_Vddd | 36 | A_Y7_DGND |
| 37 | No Connect | 38 | No Connect |
| 39 | No Connect | 40 | No Connect |
| 41 | No Connect | 42 | No Connect |
| 43 | No Connect | 44 | No Connect |

Table 18. Suggested Digital Power connector signal assignment.

4.5 ANALOG POWER CONNECTOR

The Analog Voltage connector provides analog power to the FPIX2 modules. Each connector provides analog power to one ¼ station. The operating voltage for each Vdda channel is 2.5V with 600mA maximum current. Trace widths should be wide enough to accommodate a less than 10% voltage drop over the length of trace. For ½ oz copper, the suggested trace width is 130 mil. Table 19 offers a suggested pin assignment.

| Analog Power Connector | | | |
|------------------------|-------------|-------|-------------|
| Pin # | Signal | Pin # | Signal |
| 1 | No Connect | 2 | No Connect |
| 3 | No Connect | 4 | No Connect |
| 5 | No Connect | 6 | No Connect |
| 7 | No Connect | 8 | No Connect |
| 9 | A_X1_Vdda | 10 | A_X1_AGND |
| 11 | A_X2_Vdda | 12 | A_X2_AGND |
| 13 | A_X3_Vdda | 14 | A_X3_AGND |
| 15 | A_X4_Vdda | 16 | A_X4_AGND |
| 17 | A_X5_Vdda | 18 | A_X5_AGND |
| 19 | A_X6Y8_Vdda | 20 | A_X6Y8_AGND |
| 21 | A_X7Y9_Vdda | 22 | A_X7Y9_AGND |
| 23 | A_Y1_Vdda | 24 | A_Y1_AGND |
| 25 | A_Y2_Vdda | 26 | A_Y2_AGND |
| 27 | A_Y3_Vdda | 28 | A_Y3_AGND |
| 29 | A_Y4_Vdda | 30 | A_Y4_AGND |
| 31 | A_Y5_Vdda | 32 | A_Y5_AGND |
| 33 | A_Y6_Vdda | 34 | A_Y6_AGND |
| 35 | A_Y7_Vdda | 36 | A_Y7_AGND |
| 37 | No Connect | 38 | No Connect |
| 39 | No Connect | 40 | No Connect |
| 41 | No Connect | 42 | No Connect |
| 43 | No Connect | 44 | No Connect |

Table 19. Suggested Analog Power connector signal assignment.

4.6 DIGITAL VOLTAGE SENSE CONNECTOR

The digital voltage sense connector feeds back the digital supply voltage on the FPIX2 module to the digital power supply sense. The sense signals are connected to the digital power at the FPIX2 module. Table 20 offers a suggest pin assignment for the digital voltage sense connector.

| Digital Voltage Sense Connector | | | |
|---------------------------------|---------------------|-------|------------------|
| Pin # | Signal | Pin # | Signal |
| 1 | DSense Cable Shield | 2 | No Connect |
| 3 | No Connect | 4 | No Connect |
| 5 | A_X1_DSense(+) | 6 | A_X1_DSense(-) |
| 7 | A_X2_DSense(+) | 8 | A_X2_DSense(-) |
| 9 | A_X3_DSense(+) | 10 | A_X3_DSense(-) |
| 11 | A_X4_DSense(+) | 12 | A_X4_DSense(-) |
| 13 | A_X5_DSense(+) | 14 | A_X5_DSense(-) |
| 15 | A_X6Y8_DSense(+) | 16 | A_X6Y8_DSense(-) |
| 17 | A_X7Y9_DSense(+) | 18 | A_X7Y9_DSense(-) |
| 19 | A_Y1_DSense(+) | 20 | A_Y1_DSense(-) |
| 21 | A_Y2_DSense(+) | 22 | A_Y2_DSense(-) |
| 23 | A_Y3_DSense(+) | 24 | A_Y3_DSense(-) |
| 25 | A_Y4_DSense(+) | 26 | A_Y4_DSense(-) |
| 27 | A_Y5_DSense(+) | 28 | A_Y5_DSense(-) |
| 29 | A_Y6_DSense(+) | 30 | A_Y6_DSense(-) |
| 31 | A_Y7_DSense(+) | 32 | A_Y7_DSense(-) |
| 33 | No Connect | 34 | No Connect |
| 35 | No Connect | 36 | No Connect |

Table 20. Digital voltage sense connector signal assignment.

4.7 ANALOG VOLTAGE SENSE CONNECTOR

The analog voltage sense connector feeds back the analog supply voltage on the FPIX2 module to the analog power supply sense. The sense signals are connected to the analog power at the FPIX2 module. Table 21 offers a suggest pin assignment for the analog voltage sense connector.

| Analog Voltage Sense Connector | | | |
|--------------------------------|---------------------|-------|------------------|
| Pin # | Signal | Pin # | Signal |
| 1 | ASense Cable Shield | 2 | No Connect |
| 3 | No Connect | 4 | No Connect |
| 5 | A_X1_Asense(+) | 6 | A_X1_Asense(-) |
| 7 | A_X2_Asense(+) | 8 | A_X2_Asense(-) |
| 9 | A_X3_Asense(+) | 10 | A_X3_Asense(-) |
| 11 | A_X4_Asense(+) | 12 | A_X4_Asense(-) |
| 13 | A_X5_Asense(+) | 14 | A_X5_Asense(-) |
| 15 | A_X6Y8_Asense(+) | 16 | A_X6Y8_Asense(-) |
| 17 | A_X7Y9_Asense(+) | 18 | A_X7Y9_Asense(-) |
| 19 | A_Y1_Asense(+) | 20 | A_Y1_Asense(-) |
| 21 | A_Y2_Asense(+) | 22 | A_Y2_Asense(-) |
| 23 | A_Y3_Asense(+) | 24 | A_Y3_Asense(-) |
| 25 | A_Y4_Asense(+) | 26 | A_Y4_Asense(-) |
| 27 | A_Y5_Asense(+) | 28 | A_Y5_Asense(-) |
| 29 | A_Y6_Asense(+) | 30 | A_Y6_Asense(-) |
| 31 | A_Y7_Asense(+) | 32 | A_Y7_Asense(-) |
| 33 | No Connect | 34 | No Connect |
| 35 | No Connect | 36 | No Connect |

Table 21. Analog voltage sense connector signal assignment.

4.8 CHARGE-INJECT CONNECTOR

Table 22 provides a suggested pin assignment for the charge-inject connector. Charge-inject signals are typically 1V to 2V. Board traces should be capable of carrying 40mA to accommodate a 50Ω termination.

| Charge-Inject Connector | | | |
|-------------------------|-------------------------|-------|------------------|
| Pin # | Signal | Pin # | Signal |
| 1 | Charge-Inj Cable Shield | 2 | No Connect |
| 3 | No Connect | 4 | No Connect |
| 5 | A_X1_INJECT(+) | 6 | A_X1_INJECT(-) |
| 7 | A_X2_INJECT(+) | 8 | A_X2_INJECT(-) |
| 9 | A_X3_INJECT(+) | 10 | A_X3_INJECT(-) |
| 11 | A_X4_INJECT(+) | 12 | A_X4_INJECT(-) |
| 13 | A_X5_INJECT(+) | 14 | A_X5_INJECT(-) |
| 15 | A_X6Y8_INJECT(+) | 16 | A_X6Y8_INJECT(-) |
| 17 | A_X7Y9_INJECT(+) | 18 | A_X7Y9_INJECT(-) |
| 19 | A_Y1_INJECT(+) | 20 | A_Y1_INJECT(-) |
| 21 | A_Y2_INJECT(+) | 22 | A_Y2_INJECT(-) |
| 23 | A_Y3_INJECT(+) | 24 | A_Y3_INJECT(-) |
| 25 | A_Y4_INJECT(+) | 26 | A_Y4_INJECT(-) |
| 27 | A_Y5_INJECT(+) | 28 | A_Y5_INJECT(-) |
| 29 | A_Y6_INJECT(+) | 30 | A_Y6_INJECT(-) |
| 31 | A_Y7_INJECT(+) | 32 | A_Y7_INJECT(-) |
| 33 | No Connect | 34 | No Connect |
| 35 | No Connect | 36 | No Connect |

Table 22. Charge-inject connector signal assignment.

4.9 HIGH-VOLTAGE CONNECTORS

The high-voltage connectors will provide up to 1000V DC at 10 μ A per channel. High-voltage traces should be spaced to accommodate 1000V DC. The high voltage return signals (-) can be assumed to be at 0V DC, requiring no special high-voltage spacing treatment. Tables 23 and 24 offer pin assignments for the two high-voltage connectors required for each 1/4 station.

| High Voltage Connector – A_HVI | | | |
|--------------------------------|-----------------|-------|-----------------|
| Pin # | Signal | Pin # | Signal |
| 1 | HV Cable Shield | 2 | No Connect |
| 3 | No Connect | 4 | A_X1_Vbias(-) |
| 5 | A_X2_Vbias(-) | 6 | A_X3_Vbias(-) |
| 7 | *REMOVED* | 8 | *REMOVED* |
| 9 | *REMOVED* | 10 | *REMOVED* |
| 11 | *REMOVED* | 12 | *REMOVED* |
| 13 | *REMOVED* | 14 | A_X1_Vbias(+) |
| 15 | *REMOVED* | 16 | *REMOVED* |
| 17 | A_X2_Vbias(+) | 18 | *REMOVED* |
| 19 | *REMOVED* | 20 | *REMOVED* |
| 21 | *REMOVED* | 22 | A_X3_Vbias(+) |
| 23 | *REMOVED* | 24 | *REMOVED* |
| 25 | A_X4_Vbias(+) | 26 | *REMOVED* |
| 27 | *REMOVED* | 28 | *REMOVED* |
| 29 | *REMOVED* | 30 | A_X5_Vbias(+) |
| 31 | *REMOVED* | 32 | *REMOVED* |
| 33 | A_X6Y8_Vbias(+) | 34 | *REMOVED* |
| 35 | *REMOVED* | 36 | *REMOVED* |
| 37 | *REMOVED* | 38 | A_X7Y9_Vbias(+) |
| 39 | *REMOVED* | 40 | *REMOVED* |
| 41 | *REMOVED* | 42 | *REMOVED* |
| 43 | *REMOVED* | 44 | *REMOVED* |
| 45 | A_X4_Vbias(-) | 46 | A_X5_Vbias(-) |
| 47 | A_X6Y8_Vbias(-) | 48 | A_X7Y9_Vbias(-) |

Table 23. High-voltage connector “A_HVI” signal assignment.

| High Voltage Connector – A_HV2 | | | |
|--------------------------------|-----------------|-------|---------------|
| Pin # | Signal | Pin # | Signal |
| 1 | HV Cable Shield | 2 | No Connect |
| 3 | No Connect | 4 | A_Y1_Vbias(-) |
| 5 | A_Y2_Vbias(-) | 6 | A_Y3_Vbias(-) |
| 7 | *REMOVED* | 8 | *REMOVED* |
| 9 | *REMOVED* | 10 | *REMOVED* |
| 11 | *REMOVED* | 12 | *REMOVED* |
| 13 | *REMOVED* | 14 | A_Y1_Vbias(+) |
| 15 | *REMOVED* | 16 | *REMOVED* |
| 17 | A_Y2_Vbias(+) | 18 | *REMOVED* |
| 19 | *REMOVED* | 20 | *REMOVED* |
| 21 | *REMOVED* | 22 | A_Y3_Vbias(+) |
| 23 | *REMOVED* | 24 | *REMOVED* |
| 25 | A_Y4_Vbias(+) | 26 | *REMOVED* |
| 27 | *REMOVED* | 28 | *REMOVED* |
| 29 | *REMOVED* | 30 | A_Y5_Vbias(+) |
| 31 | *REMOVED* | 32 | *REMOVED* |
| 33 | A_Y6_Vbias(+) | 34 | *REMOVED* |
| 35 | *REMOVED* | 36 | *REMOVED* |
| 37 | *REMOVED* | 38 | A_Y7_Vbias(+) |
| 39 | *REMOVED* | 40 | *REMOVED* |
| 41 | *REMOVED* | 42 | *REMOVED* |
| 43 | *REMOVED* | 44 | *REMOVED* |
| 45 | A_Y4_Vbias(-) | 46 | A_Y5_Vbias(-) |
| 47 | A_Y6_Vbias(-) | 48 | A_Y7_Vbias(-) |

Table 24. High-voltage connector “A_HV2” signal assignment.

4.10 DATA AND CONTROL CABLES

Tables 25 through 32 describe the signal assignments for the eight outside vacuum data and control connectors. Note that the signal names are of the format *GPIO* due to the lack of flex cable/module pin assignment constraints at the time of the writing of this document. The pin assignments described in this section and the next section (flex circuit connectors) are arranged to optimize the routing by minimizing the amount of possible signal collision conditions and therefore minimizing the number of routing layers required.

| <i>Connector A_D1 (connects module A_Y1)</i> | | | |
|--|----------------|--------------|----------------|
| <i>Pin #</i> | <i>Signal</i> | <i>Pin #</i> | <i>Signal</i> |
| 1 | A_Y1_GPIO34(-) | 35 | A_Y1_GPIO17(-) |
| 2 | A_Y1_GPIO34(+) | 36 | A_Y1_GPIO17(+) |
| 3 | A_Y1_GPIO33(-) | 37 | A_Y1_GPIO16(-) |
| 4 | A_Y1_GPIO33(+) | 38 | A_Y1_GPIO16(+) |
| 5 | A_Y1_GPIO32(-) | 39 | A_Y1_GPIO15(-) |
| 6 | A_Y1_GPIO32(+) | 40 | A_Y1_GPIO15(+) |
| 7 | A_Y1_GPIO31(-) | 41 | A_Y1_GPIO14(-) |
| 8 | A_Y1_GPIO31(+) | 42 | A_Y1_GPIO14(+) |
| 9 | A_Y1_GPIO30(-) | 43 | A_Y1_GPIO13(-) |
| 10 | A_Y1_GPIO30(+) | 44 | A_Y1_GPIO13(+) |
| 11 | A_Y1_GPIO29(-) | 45 | A_Y1_GPIO12(-) |
| 12 | A_Y1_GPIO29(+) | 46 | A_Y1_GPIO12(+) |
| 13 | A_Y1_GPIO28(-) | 47 | A_Y1_GPIO11(-) |
| 14 | A_Y1_GPIO28(+) | 48 | A_Y1_GPIO11(+) |
| 15 | A_Y1_GPIO27(+) | 49 | A_Y1_GPIO10(+) |
| 16 | A_Y1_GPIO27(-) | 50 | A_Y1_GPIO10(-) |
| 17 | A_Y1_GPIO26(+) | 51 | A_Y1_GPIO9(+) |
| 18 | A_Y1_GPIO26(-) | 52 | A_Y1_GPIO9(-) |
| 19 | A_Y1_GPIO25(+) | 53 | A_Y1_GPIO8(+) |
| 20 | A_Y1_GPIO25(-) | 54 | A_Y1_GPIO8(-) |
| 21 | A_Y1_GPIO24(+) | 55 | A_Y1_GPIO7(+) |
| 22 | A_Y1_GPIO24(-) | 56 | A_Y1_GPIO7(-) |
| 23 | A_Y1_GPIO23(-) | 57 | A_Y1_GPIO6(-) |
| 24 | A_Y1_GPIO23(+) | 58 | A_Y1_GPIO6(+) |
| 25 | A_Y1_GPIO22(+) | 59 | A_Y1_GPIO5(+) |
| 26 | A_Y1_GPIO22(-) | 60 | A_Y1_GPIO5(-) |
| 27 | A_Y1_GPIO21(+) | 61 | A_Y1_GPIO4(+) |
| 28 | A_Y1_GPIO21(-) | 62 | A_Y1_GPIO4(-) |
| 29 | A_Y1_GPIO20(+) | 63 | A_Y1_GPIO3(+) |
| 30 | A_Y1_GPIO20(-) | 64 | A_Y1_GPIO3(-) |
| 31 | A_Y1_GPIO19(+) | 65 | A_Y1_GPIO2(+) |
| 32 | A_Y1_GPIO19(-) | 66 | A_Y1_GPIO2(-) |
| 33 | A_Y1_GPIO18(-) | 67 | A_Y1_GPIO1(-) |
| 34 | A_Y1_GPIO18(+) | 68 | A_Y1_GPIO1(+) |

Table 25. Data connector “A_D1” pin assignment.

Connector A_D2 (connects module A_Y2 and part A_Y3)

| <i>Pin #</i> | <i>Signal</i> | <i>Pin #</i> | <i>Signal</i> |
|--------------|----------------|--------------|----------------|
| 1 | A_Y2_GPIO16(+) | 35 | A_Y2_GPIO1(+) |
| 2 | A_Y2_GPIO16(-) | 36 | A_Y2_GPIO1(-) |
| 3 | A_Y2_GPIO17(+) | 37 | A_Y2_GPIO2(+) |
| 4 | A_Y2_GPIO17(-) | 38 | A_Y2_GPIO2(-) |
| 5 | A_Y2_GPIO18(+) | 39 | A_Y2_GPIO3(+) |
| 6 | A_Y2_GPIO18(-) | 40 | A_Y2_GPIO3(-) |
| 7 | A_Y2_GPIO19(+) | 41 | A_Y2_GPIO4(+) |
| 8 | A_Y2_GPIO19(-) | 42 | A_Y2_GPIO4(-) |
| 9 | A_Y2_GPIO20(+) | 43 | A_Y2_GPIO5(+) |
| 10 | A_Y2_GPIO20(-) | 44 | A_Y2_GPIO5(-) |
| 11 | A_Y2_GPIO21(+) | 45 | A_Y2_GPIO6(+) |
| 12 | A_Y2_GPIO21(-) | 46 | A_Y2_GPIO6(-) |
| 13 | A_Y2_GPIO22(+) | 47 | A_Y2_GPIO7(+) |
| 14 | A_Y2_GPIO22(-) | 48 | A_Y2_GPIO7(-) |
| 15 | A_Y2_GPIO23(+) | 49 | A_Y2_GPIO8(+) |
| 16 | A_Y2_GPIO23(-) | 50 | A_Y2_GPIO8(-) |
| 17 | A_Y2_GPIO24(+) | 51 | A_Y2_GPIO9(+) |
| 18 | A_Y2_GPIO24(-) | 52 | A_Y2_GPIO9(-) |
| 19 | A_Y2_GPIO25(+) | 53 | A_Y2_GPIO10(+) |
| 20 | A_Y2_GPIO25(-) | 54 | A_Y2_GPIO10(-) |
| 21 | A_Y2_GPIO26(+) | 55 | A_Y2_GPIO11(+) |
| 22 | A_Y2_GPIO26(-) | 56 | A_Y2_GPIO11(-) |
| 23 | A_Y2_GPIO27(+) | 57 | A_Y2_GPIO12(+) |
| 24 | A_Y2_GPIO27(-) | 58 | A_Y2_GPIO12(-) |
| 25 | A_Y2_GPIO28(+) | 59 | A_Y2_GPIO13(+) |
| 26 | A_Y2_GPIO28(-) | 60 | A_Y2_GPIO13(-) |
| 27 | A_Y2_GPIO29(+) | 61 | A_Y2_GPIO14(+) |
| 28 | A_Y2_GPIO29(-) | 62 | A_Y2_GPIO14(-) |
| 29 | A_Y2_GPIO30(+) | 63 | A_Y2_GPIO15(+) |
| 30 | A_Y2_GPIO30(-) | 64 | A_Y2_GPIO15(-) |
| 31 | A_Y3_GPIO30(-) | 65 | A_Y3_GPIO15(-) |
| 32 | A_Y3_GPIO30(+) | 66 | A_Y3_GPIO15(+) |
| 33 | A_Y3_GPIO29(-) | 67 | A_Y3_GPIO14(-) |
| 34 | A_Y3_GPIO29(+) | 68 | A_Y3_GPIO14(+) |

Table 26. Data connector “A_D2” pin assignment.

Connector A_D3 (connects module A_Y4 and A_Y7)

| <i>Pin #</i> | <i>Signal</i> | <i>Pin #</i> | <i>Signal</i> |
|--------------|----------------|--------------|----------------|
| 1 | A_Y4_GPIO13(+) | 51 | A_Y4_GPIO1(+) |
| 2 | A_Y4_GPIO13(-) | 52 | A_Y4_GPIO1(-) |
| 3 | A_Y4_GPIO14(+) | 53 | A_Y4_GPIO2(+) |
| 4 | A_Y4_GPIO14(-) | 54 | A_Y4_GPIO2(-) |
| 5 | A_Y4_GPIO15(+) | 55 | A_Y4_GPIO3(+) |
| 6 | A_Y4_GPIO15(-) | 56 | A_Y4_GPIO3(-) |
| 7 | A_Y4_GPIO16(+) | 57 | A_Y4_GPIO4(+) |
| 8 | A_Y4_GPIO16(-) | 58 | A_Y4_GPIO4(-) |
| 9 | A_Y4_GPIO17(+) | 59 | A_Y4_GPIO5(+) |
| 10 | A_Y4_GPIO17(-) | 60 | A_Y4_GPIO5(-) |
| 11 | A_Y4_GPIO18(+) | 61 | A_Y4_GPIO6(+) |
| 12 | A_Y4_GPIO18(-) | 62 | A_Y4_GPIO6(-) |
| 13 | A_Y4_GPIO19(+) | 63 | A_Y4_GPIO7(+) |
| 14 | A_Y4_GPIO19(-) | 64 | A_Y4_GPIO7(-) |
| 15 | A_Y4_GPIO20(+) | 65 | A_Y4_GPIO8(+) |
| 16 | A_Y4_GPIO20(-) | 66 | A_Y4_GPIO8(-) |
| 17 | A_Y4_GPIO21(+) | 67 | A_Y4_GPIO9(+) |
| 18 | A_Y4_GPIO21(-) | 68 | A_Y4_GPIO9(-) |
| 19 | A_Y4_GPIO22(+) | 69 | A_Y4_GPIO10(+) |
| 20 | A_Y4_GPIO22(-) | 70 | A_Y4_GPIO10(-) |
| 21 | A_Y4_GPIO23(+) | 71 | A_Y4_GPIO11(+) |
| 22 | A_Y4_GPIO23(-) | 72 | A_Y4_GPIO11(-) |
| 23 | A_Y4_GPIO24(+) | 73 | A_Y4_GPIO12(+) |
| 24 | A_Y4_GPIO24(-) | 74 | A_Y4_GPIO12(-) |
| 25 | | 75 | |
| 26 | | 76 | |
| 27 | A_Y7_GPIO24(-) | 77 | A_Y7_GPIO12(-) |
| 28 | A_Y7_GPIO24(+) | 78 | A_Y7_GPIO12(+) |
| 29 | A_Y7_GPIO23(-) | 79 | A_Y7_GPIO11(-) |
| 30 | A_Y7_GPIO23(+) | 80 | A_Y7_GPIO11(+) |
| 31 | A_Y7_GPIO22(-) | 81 | A_Y7_GPIO10(-) |
| 32 | A_Y7_GPIO22(+) | 82 | A_Y7_GPIO10(+) |
| 33 | A_Y7_GPIO21(-) | 83 | A_Y7_GPIO9(-) |
| 34 | A_Y7_GPIO21(+) | 84 | A_Y7_GPIO9(+) |
| 35 | A_Y7_GPIO20(-) | 85 | A_Y7_GPIO8(-) |
| 36 | A_Y7_GPIO20(+) | 86 | A_Y7_GPIO8(+) |
| 37 | A_Y7_GPIO19(-) | 87 | A_Y7_GPIO7(-) |
| 38 | A_Y7_GPIO19(+) | 88 | A_Y7_GPIO7(+) |
| 39 | A_Y7_GPIO18(-) | 89 | A_Y7_GPIO6(-) |
| 40 | A_Y7_GPIO18(+) | 90 | A_Y7_GPIO6(+) |
| 41 | A_Y7_GPIO17(-) | 91 | A_Y7_GPIO5(-) |
| 42 | A_Y7_GPIO17(+) | 92 | A_Y7_GPIO5(+) |
| 43 | A_Y7_GPIO16(-) | 93 | A_Y7_GPIO4(-) |
| 44 | A_Y7_GPIO16(+) | 94 | A_Y7_GPIO4(+) |
| 45 | A_Y7_GPIO15(-) | 95 | A_Y7_GPIO3(-) |
| 46 | A_Y7_GPIO15(+) | 96 | A_Y7_GPIO3(+) |
| 47 | A_Y7_GPIO14(-) | 97 | A_Y7_GPIO2(-) |
| 48 | A_Y7_GPIO14(+) | 98 | A_Y7_GPIO2(+) |
| 49 | A_Y7_GPIO13(-) | 99 | A_Y7_GPIO1(-) |
| 50 | A_Y7_GPIO13(+) | 100 | A_Y7_GPIO1(+) |

Table 27. Data connector “A_D3” pin assignment.

Connector A_D4 (connects module A_Y5 and A_X6/A_Y8)

| <i>Pin #</i> | <i>Signal</i> | <i>Pin #</i> | <i>Signal</i> |
|--------------|------------------|--------------|------------------|
| 1 | A_Y5_GPIO24(-) | 51 | A_Y5_GPIO12(-) |
| 2 | A_Y5_GPIO24(+) | 52 | A_Y5_GPIO12(+) |
| 3 | A_Y5_GPIO23(-) | 53 | A_Y5_GPIO11(-) |
| 4 | A_Y5_GPIO23(+) | 54 | A_Y5_GPIO11(+) |
| 5 | A_Y5_GPIO22(-) | 55 | A_Y5_GPIO10(-) |
| 6 | A_Y5_GPIO22(+) | 56 | A_Y5_GPIO10(+) |
| 7 | A_Y5_GPIO21(-) | 57 | A_Y5_GPIO9(-) |
| 8 | A_Y5_GPIO21(+) | 58 | A_Y5_GPIO9(+) |
| 9 | A_Y5_GPIO20(-) | 59 | A_Y5_GPIO8(-) |
| 10 | A_Y5_GPIO20(+) | 60 | A_Y5_GPIO8(+) |
| 11 | A_Y5_GPIO19(-) | 61 | A_Y5_GPIO7(-) |
| 12 | A_Y5_GPIO19(+) | 62 | A_Y5_GPIO7(+) |
| 13 | A_Y5_GPIO18(-) | 63 | A_Y5_GPIO6(-) |
| 14 | A_Y5_GPIO18(+) | 64 | A_Y5_GPIO6(+) |
| 15 | A_Y5_GPIO17(-) | 65 | A_Y5_GPIO5(-) |
| 16 | A_Y5_GPIO17(+) | 66 | A_Y5_GPIO5(+) |
| 17 | A_Y5_GPIO16(-) | 67 | A_Y5_GPIO4(-) |
| 18 | A_Y5_GPIO16(+) | 68 | A_Y5_GPIO4(+) |
| 19 | A_Y5_GPIO15(-) | 69 | A_Y5_GPIO3(-) |
| 20 | A_Y5_GPIO15(+) | 70 | A_Y5_GPIO3(+) |
| 21 | A_Y5_GPIO14(-) | 71 | A_Y5_GPIO2(-) |
| 22 | A_Y5_GPIO14(+) | 72 | A_Y5_GPIO2(+) |
| 23 | A_Y5_GPIO13(-) | 73 | A_Y5_GPIO1(-) |
| 24 | A_Y5_GPIO13(+) | 74 | A_Y5_GPIO1(+) |
| 25 | | 75 | |
| 26 | | 76 | |
| 27 | A_X6Y8_GPIO13(+) | 77 | A_X6Y8_GPIO1(+) |
| 28 | A_X6Y8_GPIO13(-) | 78 | A_X6Y8_GPIO1(-) |
| 29 | A_X6Y8_GPIO14(+) | 79 | A_X6Y8_GPIO2(+) |
| 30 | A_X6Y8_GPIO14(-) | 80 | A_X6Y8_GPIO2(-) |
| 31 | A_X6Y8_GPIO15(+) | 81 | A_X6Y8_GPIO3(+) |
| 32 | A_X6Y8_GPIO15(-) | 82 | A_X6Y8_GPIO3(-) |
| 33 | A_X6Y8_GPIO16(+) | 83 | A_X6Y8_GPIO4(+) |
| 34 | A_X6Y8_GPIO16(-) | 84 | A_X6Y8_GPIO4(-) |
| 35 | A_X6Y8_GPIO17(+) | 85 | A_X6Y8_GPIO5(+) |
| 36 | A_X6Y8_GPIO17(-) | 86 | A_X6Y8_GPIO5(-) |
| 37 | A_X6Y8_GPIO18(+) | 87 | A_X6Y8_GPIO6(+) |
| 38 | A_X6Y8_GPIO18(-) | 88 | A_X6Y8_GPIO6(-) |
| 39 | A_X6Y8_GPIO19(+) | 89 | A_X6Y8_GPIO7(+) |
| 40 | A_X6Y8_GPIO19(-) | 90 | A_X6Y8_GPIO7(-) |
| 41 | A_X6Y8_GPIO20(+) | 91 | A_X6Y8_GPIO8(+) |
| 42 | A_X6Y8_GPIO20(-) | 92 | A_X6Y8_GPIO8(-) |
| 43 | A_X6Y8_GPIO21(+) | 93 | A_X6Y8_GPIO9(+) |
| 44 | A_X6Y8_GPIO21(-) | 94 | A_X6Y8_GPIO9(-) |
| 45 | A_X6Y8_GPIO22(+) | 95 | A_X6Y8_GPIO10(+) |
| 46 | A_X6Y8_GPIO22(-) | 96 | A_X6Y8_GPIO10(-) |
| 47 | A_X6Y8_GPIO23(+) | 97 | A_X6Y8_GPIO11(+) |
| 48 | A_X6Y8_GPIO23(-) | 98 | A_X6Y8_GPIO11(-) |
| 49 | A_X6Y8_GPIO24(+) | 99 | A_X6Y8_GPIO12(+) |
| 50 | A_X6Y8_GPIO24(-) | 100 | A_X6Y8_GPIO12(-) |

Table 28. Data connector “A_D4” pin assignment.

Connector A_D5 (connects module A_Y3(most) and A_Y6)

| <i>Pin #</i> | <i>Signal</i> | <i>Pin #</i> | <i>Signal</i> |
|--------------|----------------|--------------|----------------|
| 1 | A_Y3_GPIO28(-) | 51 | A_Y3_GPIO13(-) |
| 2 | A_Y3_GPIO28(+) | 52 | A_Y3_GPIO13(+) |
| 3 | A_Y3_GPIO27(-) | 53 | A_Y3_GPIO12(-) |
| 4 | A_Y3_GPIO27(+) | 54 | A_Y3_GPIO12(+) |
| 5 | A_Y3_GPIO26(-) | 55 | A_Y3_GPIO11(-) |
| 6 | A_Y3_GPIO26(+) | 56 | A_Y3_GPIO11(+) |
| 7 | A_Y3_GPIO25(-) | 57 | A_Y3_GPIO10(-) |
| 8 | A_Y3_GPIO25(+) | 58 | A_Y3_GPIO10(+) |
| 9 | A_Y3_GPIO24(-) | 59 | A_Y3_GPIO9(-) |
| 10 | A_Y3_GPIO24(+) | 60 | A_Y3_GPIO9(+) |
| 11 | A_Y3_GPIO23(-) | 61 | A_Y3_GPIO8(-) |
| 12 | A_Y3_GPIO23(+) | 62 | A_Y3_GPIO8(+) |
| 13 | A_Y3_GPIO22(-) | 63 | A_Y3_GPIO7(-) |
| 14 | A_Y3_GPIO22(+) | 64 | A_Y3_GPIO7(+) |
| 15 | A_Y3_GPIO21(-) | 65 | A_Y3_GPIO6(-) |
| 16 | A_Y3_GPIO21(+) | 66 | A_Y3_GPIO6(+) |
| 17 | A_Y3_GPIO20(-) | 67 | A_Y3_GPIO5(-) |
| 18 | A_Y3_GPIO20(+) | 68 | A_Y3_GPIO5(+) |
| 19 | A_Y3_GPIO19(-) | 69 | A_Y3_GPIO4(-) |
| 20 | A_Y3_GPIO19(+) | 70 | A_Y3_GPIO4(+) |
| 21 | A_Y3_GPIO18(-) | 71 | A_Y3_GPIO3(-) |
| 22 | A_Y3_GPIO18(+) | 72 | A_Y3_GPIO3(+) |
| 23 | A_Y3_GPIO17(-) | 73 | A_Y3_GPIO2(-) |
| 24 | A_Y3_GPIO17(+) | 74 | A_Y3_GPIO2(+) |
| 25 | A_Y3_GPIO16(-) | 75 | A_Y3_GPIO1(-) |
| 26 | A_Y3_GPIO16(+) | 76 | A_Y3_GPIO1(+) |
| 27 | A_Y6_GPIO13(+) | 77 | A_Y6_GPIO1(+) |
| 28 | A_Y6_GPIO13(-) | 78 | A_Y6_GPIO1(-) |
| 29 | A_Y6_GPIO14(+) | 79 | A_Y6_GPIO2(+) |
| 30 | A_Y6_GPIO14(-) | 80 | A_Y6_GPIO2(-) |
| 31 | A_Y6_GPIO15(+) | 81 | A_Y6_GPIO3(+) |
| 32 | A_Y6_GPIO15(-) | 82 | A_Y6_GPIO3(-) |
| 33 | A_Y6_GPIO16(+) | 83 | A_Y6_GPIO4(+) |
| 34 | A_Y6_GPIO16(-) | 84 | A_Y6_GPIO4(-) |
| 35 | A_Y6_GPIO17(+) | 85 | A_Y6_GPIO5(+) |
| 36 | A_Y6_GPIO17(-) | 86 | A_Y6_GPIO5(-) |
| 37 | A_Y6_GPIO18(+) | 87 | A_Y6_GPIO6(+) |
| 38 | A_Y6_GPIO18(-) | 88 | A_Y6_GPIO6(-) |
| 39 | A_Y6_GPIO19(+) | 89 | A_Y6_GPIO7(+) |
| 40 | A_Y6_GPIO19(-) | 90 | A_Y6_GPIO7(-) |
| 41 | A_Y6_GPIO20(+) | 91 | A_Y6_GPIO8(+) |
| 42 | A_Y6_GPIO20(-) | 92 | A_Y6_GPIO8(-) |
| 43 | A_Y6_GPIO21(+) | 93 | A_Y6_GPIO9(+) |
| 44 | A_Y6_GPIO21(-) | 94 | A_Y6_GPIO9(-) |
| 45 | A_Y6_GPIO22(+) | 95 | A_Y6_GPIO10(+) |
| 46 | A_Y6_GPIO22(-) | 96 | A_Y6_GPIO10(-) |
| 47 | A_Y6_GPIO23(+) | 97 | A_Y6_GPIO11(+) |
| 48 | A_Y6_GPIO23(-) | 98 | A_Y6_GPIO11(-) |
| 49 | A_Y6_GPIO24(+) | 99 | A_Y6_GPIO12(+) |
| 50 | A_Y6_GPIO24(-) | 100 | A_Y6_GPIO12(-) |

Table 29. Data connector “A_D5” pin assignment.

Connector A_D6 (connects module A_X1 and A_X4)

| <i>Pin #</i> | <i>Signal</i> | <i>Pin #</i> | <i>Signal</i> |
|--------------|----------------|--------------|----------------|
| 1 | A_X1_GPIO24(-) | 51 | A_X1_GPIO12(-) |
| 2 | A_X1_GPIO24(+) | 52 | A_X1_GPIO12(+) |
| 3 | A_X1_GPIO23(-) | 53 | A_X1_GPIO11(-) |
| 4 | A_X1_GPIO23(+) | 54 | A_X1_GPIO11(+) |
| 5 | A_X1_GPIO22(-) | 55 | A_X1_GPIO10(-) |
| 6 | A_X1_GPIO22(+) | 56 | A_X1_GPIO10(+) |
| 7 | A_X1_GPIO21(-) | 57 | A_X1_GPIO9(-) |
| 8 | A_X1_GPIO21(+) | 58 | A_X1_GPIO9(+) |
| 9 | A_X1_GPIO20(-) | 59 | A_X1_GPIO8(-) |
| 10 | A_X1_GPIO20(+) | 60 | A_X1_GPIO8(+) |
| 11 | A_X1_GPIO19(-) | 61 | A_X1_GPIO7(-) |
| 12 | A_X1_GPIO19(+) | 62 | A_X1_GPIO7(+) |
| 13 | A_X1_GPIO18(-) | 63 | A_X1_GPIO6(-) |
| 14 | A_X1_GPIO18(+) | 64 | A_X1_GPIO6(+) |
| 15 | A_X1_GPIO17(-) | 65 | A_X1_GPIO5(-) |
| 16 | A_X1_GPIO17(+) | 66 | A_X1_GPIO5(+) |
| 17 | A_X1_GPIO16(-) | 67 | A_X1_GPIO4(-) |
| 18 | A_X1_GPIO16(+) | 68 | A_X1_GPIO4(+) |
| 19 | A_X1_GPIO15(-) | 69 | A_X1_GPIO3(-) |
| 20 | A_X1_GPIO15(+) | 70 | A_X1_GPIO3(+) |
| 21 | A_X1_GPIO14(-) | 71 | A_X1_GPIO2(-) |
| 22 | A_X1_GPIO14(+) | 72 | A_X1_GPIO2(+) |
| 23 | A_X1_GPIO13(-) | 73 | A_X1_GPIO1(-) |
| 24 | A_X1_GPIO13(+) | 74 | A_X1_GPIO1(+) |
| 25 | | 75 | |
| 26 | | 76 | |
| 27 | A_X4_GPIO13(+) | 77 | A_X4_GPIO1(+) |
| 28 | A_X4_GPIO13(-) | 78 | A_X4_GPIO1(-) |
| 29 | A_X4_GPIO14(+) | 79 | A_X4_GPIO2(+) |
| 30 | A_X4_GPIO14(-) | 80 | A_X4_GPIO2(-) |
| 31 | A_X4_GPIO15(+) | 81 | A_X4_GPIO3(+) |
| 32 | A_X4_GPIO15(-) | 82 | A_X4_GPIO3(-) |
| 33 | A_X4_GPIO16(+) | 83 | A_X4_GPIO4(+) |
| 34 | A_X4_GPIO16(-) | 84 | A_X4_GPIO4(-) |
| 35 | A_X4_GPIO17(+) | 85 | A_X4_GPIO5(+) |
| 36 | A_X4_GPIO17(-) | 86 | A_X4_GPIO5(-) |
| 37 | A_X4_GPIO18(+) | 87 | A_X4_GPIO6(+) |
| 38 | A_X4_GPIO18(-) | 88 | A_X4_GPIO6(-) |
| 39 | A_X4_GPIO19(+) | 89 | A_X4_GPIO7(+) |
| 40 | A_X4_GPIO19(-) | 90 | A_X4_GPIO7(-) |
| 41 | A_X4_GPIO20(+) | 91 | A_X4_GPIO8(+) |
| 42 | A_X4_GPIO20(-) | 92 | A_X4_GPIO8(-) |
| 43 | A_X4_GPIO21(+) | 93 | A_X4_GPIO9(+) |
| 44 | A_X4_GPIO21(-) | 94 | A_X4_GPIO9(-) |
| 45 | A_X4_GPIO22(+) | 95 | A_X4_GPIO10(+) |
| 46 | A_X4_GPIO22(-) | 96 | A_X4_GPIO10(-) |
| 47 | A_X4_GPIO23(+) | 97 | A_X4_GPIO11(+) |
| 48 | A_X4_GPIO23(-) | 98 | A_X4_GPIO11(-) |
| 49 | A_X4_GPIO24(+) | 99 | A_X4_GPIO12(+) |
| 50 | A_X4_GPIO24(-) | 100 | A_X4_GPIO12(-) |

Table 30. Data connector “A_D6” pin assignment.

Connector A_D7 (connects module A_X2 and A_X5)

| <i>Pin #</i> | <i>Signal</i> | <i>Pin #</i> | <i>Signal</i> |
|--------------|----------------|--------------|----------------|
| 1 | A_X2_GPIO13(+) | 51 | A_X2_GPIO1(+) |
| 2 | A_X2_GPIO13(-) | 52 | A_X2_GPIO1(-) |
| 3 | A_X2_GPIO14(+) | 53 | A_X2_GPIO2(+) |
| 4 | A_X2_GPIO14(-) | 54 | A_X2_GPIO2(-) |
| 5 | A_X2_GPIO15(+) | 55 | A_X2_GPIO3(+) |
| 6 | A_X2_GPIO15(-) | 56 | A_X2_GPIO3(-) |
| 7 | A_X2_GPIO16(+) | 57 | A_X2_GPIO4(+) |
| 8 | A_X2_GPIO16(-) | 58 | A_X2_GPIO4(-) |
| 9 | A_X2_GPIO17(+) | 59 | A_X2_GPIO5(+) |
| 10 | A_X2_GPIO17(-) | 60 | A_X2_GPIO5(-) |
| 11 | A_X2_GPIO18(+) | 61 | A_X2_GPIO6(+) |
| 12 | A_X2_GPIO18(-) | 62 | A_X2_GPIO6(-) |
| 13 | A_X2_GPIO19(+) | 63 | A_X2_GPIO7(+) |
| 14 | A_X2_GPIO19(-) | 64 | A_X2_GPIO7(-) |
| 15 | A_X2_GPIO20(+) | 65 | A_X2_GPIO8(+) |
| 16 | A_X2_GPIO20(-) | 66 | A_X2_GPIO8(-) |
| 17 | A_X2_GPIO21(+) | 67 | A_X2_GPIO9(+) |
| 18 | A_X2_GPIO21(-) | 68 | A_X2_GPIO9(-) |
| 19 | A_X2_GPIO22(+) | 69 | A_X2_GPIO10(+) |
| 20 | A_X2_GPIO22(-) | 70 | A_X2_GPIO10(-) |
| 21 | A_X2_GPIO23(+) | 71 | A_X2_GPIO11(+) |
| 22 | A_X2_GPIO23(-) | 72 | A_X2_GPIO11(-) |
| 23 | A_X2_GPIO24(+) | 73 | A_X2_GPIO12(+) |
| 24 | A_X2_GPIO24(-) | 74 | A_X2_GPIO12(-) |
| 25 | | 75 | |
| 26 | | 76 | |
| 27 | A_X5_GPIO24(-) | 77 | A_X5_GPIO12(-) |
| 28 | A_X5_GPIO24(+) | 78 | A_X5_GPIO12(+) |
| 29 | A_X5_GPIO23(-) | 79 | A_X5_GPIO11(-) |
| 30 | A_X5_GPIO23(+) | 80 | A_X5_GPIO11(+) |
| 31 | A_X5_GPIO22(-) | 81 | A_X5_GPIO10(-) |
| 32 | A_X5_GPIO22(+) | 82 | A_X5_GPIO10(+) |
| 33 | A_X5_GPIO21(-) | 83 | A_X5_GPIO9(-) |
| 34 | A_X5_GPIO21(+) | 84 | A_X5_GPIO9(+) |
| 35 | A_X5_GPIO20(-) | 85 | A_X5_GPIO8(-) |
| 36 | A_X5_GPIO20(+) | 86 | A_X5_GPIO8(+) |
| 37 | A_X5_GPIO19(-) | 87 | A_X5_GPIO7(-) |
| 38 | A_X5_GPIO19(+) | 88 | A_X5_GPIO7(+) |
| 39 | A_X5_GPIO18(-) | 89 | A_X5_GPIO6(-) |
| 40 | A_X5_GPIO18(+) | 90 | A_X5_GPIO6(+) |
| 41 | A_X5_GPIO17(-) | 91 | A_X5_GPIO5(-) |
| 42 | A_X5_GPIO17(+) | 92 | A_X5_GPIO5(+) |
| 43 | A_X5_GPIO16(-) | 93 | A_X5_GPIO4(-) |
| 44 | A_X5_GPIO16(+) | 94 | A_X5_GPIO4(+) |
| 45 | A_X5_GPIO15(-) | 95 | A_X5_GPIO3(-) |
| 46 | A_X5_GPIO15(+) | 96 | A_X5_GPIO3(+) |
| 47 | A_X5_GPIO14(-) | 97 | A_X5_GPIO2(-) |
| 48 | A_X5_GPIO14(+) | 98 | A_X5_GPIO2(+) |
| 49 | A_X5_GPIO13(-) | 99 | A_X5_GPIO1(-) |
| 50 | A_X5_GPIO13(+) | 100 | A_X5_GPIO1(+) |

Table 31. Data connector “A_D7” pin assignment.

Connector A_D8 (connects module A_X3 and A_X7/A_Y9)

| <i>Pin #</i> | <i>Signal</i> | <i>Pin #</i> | <i>Signal</i> |
|--------------|------------------|--------------|------------------|
| 1 | A_X7Y9_GPIO24(-) | 51 | A_X7Y9_GPIO12(-) |
| 2 | A_X7Y9_GPIO24(+) | 52 | A_X7Y9_GPIO12(+) |
| 3 | A_X7Y9_GPIO23(-) | 53 | A_X7Y9_GPIO11(-) |
| 4 | A_X7Y9_GPIO23(+) | 54 | A_X7Y9_GPIO11(+) |
| 5 | A_X7Y9_GPIO22(-) | 55 | A_X7Y9_GPIO10(-) |
| 6 | A_X7Y9_GPIO22(+) | 56 | A_X7Y9_GPIO10(+) |
| 7 | A_X7Y9_GPIO21(-) | 57 | A_X7Y9_GPIO9(-) |
| 8 | A_X7Y9_GPIO21(+) | 58 | A_X7Y9_GPIO9(+) |
| 9 | A_X7Y9_GPIO20(-) | 59 | A_X7Y9_GPIO8(-) |
| 10 | A_X7Y9_GPIO20(+) | 60 | A_X7Y9_GPIO8(+) |
| 11 | A_X7Y9_GPIO19(-) | 61 | A_X7Y9_GPIO7(-) |
| 12 | A_X7Y9_GPIO19(+) | 62 | A_X7Y9_GPIO7(+) |
| 13 | A_X7Y9_GPIO18(-) | 63 | A_X7Y9_GPIO6(-) |
| 14 | A_X7Y9_GPIO18(+) | 64 | A_X7Y9_GPIO6(+) |
| 15 | A_X7Y9_GPIO17(-) | 65 | A_X7Y9_GPIO5(-) |
| 16 | A_X7Y9_GPIO17(+) | 66 | A_X7Y9_GPIO5(+) |
| 17 | A_X7Y9_GPIO16(-) | 67 | A_X7Y9_GPIO4(-) |
| 18 | A_X7Y9_GPIO16(+) | 68 | A_X7Y9_GPIO4(+) |
| 19 | A_X7Y9_GPIO15(-) | 69 | A_X7Y9_GPIO3(-) |
| 20 | A_X7Y9_GPIO15(+) | 70 | A_X7Y9_GPIO3(+) |
| 21 | A_X7Y9_GPIO14(-) | 71 | A_X7Y9_GPIO2(-) |
| 22 | A_X7Y9_GPIO14(+) | 72 | A_X7Y9_GPIO2(+) |
| 23 | A_X7Y9_GPIO13(-) | 73 | A_X7Y9_GPIO1(-) |
| 24 | A_X7Y9_GPIO13(+) | 74 | A_X7Y9_GPIO1(+) |
| 25 | | 75 | |
| 26 | | 76 | |
| 27 | A_X3_GPIO24(-) | 77 | A_X3_GPIO12(-) |
| 28 | A_X3_GPIO24(+) | 78 | A_X3_GPIO12(+) |
| 29 | A_X3_GPIO23(-) | 79 | A_X3_GPIO11(-) |
| 30 | A_X3_GPIO23(+) | 80 | A_X3_GPIO11(+) |
| 31 | A_X3_GPIO22(-) | 81 | A_X3_GPIO10(-) |
| 32 | A_X3_GPIO22(+) | 82 | A_X3_GPIO10(+) |
| 33 | A_X3_GPIO21(-) | 83 | A_X3_GPIO9(-) |
| 34 | A_X3_GPIO21(+) | 84 | A_X3_GPIO9(+) |
| 35 | A_X3_GPIO20(-) | 85 | A_X3_GPIO8(-) |
| 36 | A_X3_GPIO20(+) | 86 | A_X3_GPIO8(+) |
| 37 | A_X3_GPIO19(-) | 87 | A_X3_GPIO7(-) |
| 38 | A_X3_GPIO19(+) | 88 | A_X3_GPIO7(+) |
| 39 | A_X3_GPIO18(-) | 89 | A_X3_GPIO6(-) |
| 40 | A_X3_GPIO18(+) | 90 | A_X3_GPIO6(+) |
| 41 | A_X3_GPIO17(-) | 91 | A_X3_GPIO5(-) |
| 42 | A_X3_GPIO17(+) | 92 | A_X3_GPIO5(+) |
| 43 | A_X3_GPIO16(-) | 93 | A_X3_GPIO4(-) |
| 44 | A_X3_GPIO16(+) | 94 | A_X3_GPIO4(+) |
| 45 | A_X3_GPIO15(-) | 95 | A_X3_GPIO3(-) |
| 46 | A_X3_GPIO15(+) | 96 | A_X3_GPIO3(+) |
| 47 | A_X3_GPIO14(-) | 97 | A_X3_GPIO2(-) |
| 48 | A_X3_GPIO14(+) | 98 | A_X3_GPIO2(+) |
| 49 | A_X3_GPIO13(-) | 99 | A_X3_GPIO1(-) |
| 50 | A_X3_GPIO13(+) | 100 | A_X3_GPIO1(+) |

Table 32. Data connector “A_D8” pin assignment.

4.11 FLEX_CIRCUIT CONNECTORS

Tables 33 to 48 describe the pin assignments for the 16 flex circuit connectors inside the vacuum for one $\frac{1}{4}$ station. One flex-circuit connector connects one FPIX2 module. Note that the signal names are of the format *GPIO* due to the lack of flex cable/module pin assignment constraints at the time of the writing of this document. The pin assignments described in this section and the previous section (data and control connectors) are arranged to optimize the routing by minimizing the amount of possible signal collision conditions and therefore minimizing the number of routing layers required.

The reason the signal assignment being mirrored on the horizontal from connector N to N+1 is due to the module front-side/back-side substrate attachment geometry (see section 2.3). The two flex circuits used for connecting modules A_X1 and A_X2 (for example) will be upside-down relative to each other. Provisions should be made on the flex circuit to solder a mating connector to either the front or back side of the flex-circuit. This “upside-down” effect between connector N and N+1 manifests itself as a mirrored signal assignment between the two connectors.

| Flex-Circuit Connector A_X1 <i>(connects module X1_TL, X1_BR, X1_TR or X1_BL)</i> | | | |
|---|----------------|--------------|----------------|
| <i>Pin #</i> | <i>Signal</i> | <i>Pin #</i> | <i>Signal</i> |
| 1 | A_X1_Vbias(+) | 41 | A_X1_Vbias(-) |
| 2 | *REMOVED* | 42 | *NO CONNECT* |
| 3 | *REMOVED* | 43 | *NO CONNECT* |
| 4 | *REMOVED* | 44 | *NO CONNECT* |
| 5 | *REMOVED* | 45 | *NO CONNECT* |
| 6 | *REMOVED* | 46 | A_X1_INJECT(+) |
| 7 | *REMOVED* | 47 | A_X1_INJECT(-) |
| 8 | A_X1_DGND | 48 | A_X1_AGND |
| 9 | A_X1_Vddd | 49 | A_X1_Vdda |
| 10 | A_X1_Vddd | 50 | A_X1_Vdda |
| 11 | A_X1_Vddd | 51 | A_X1_Vdda |
| 12 | A_X1_DSense(+) | 52 | A_X1_ASense(+) |
| 13 | A_X1_DSense(-) | 53 | A_X1_ASense(-) |
| 14 | A_X1_DGND | 54 | A_X1_AGND |
| 15 | A_X1_DGND | 55 | A_X1_AGND |
| 16 | A_X1_DGND | 56 | A_X1_AGND |
| 17 | A_X1_GPIO1(+) | 57 | A_X1_GPIO13(+) |
| 18 | A_X1_GPIO1(-) | 58 | A_X1_GPIO13(-) |
| 19 | A_X1_GPIO2(+) | 59 | A_X1_GPIO14(+) |
| 20 | A_X1_GPIO2(-) | 60 | A_X1_GPIO14(-) |
| 21 | A_X1_GPIO3(+) | 61 | A_X1_GPIO15(+) |
| 22 | A_X1_GPIO3(-) | 62 | A_X1_GPIO15(-) |
| 23 | A_X1_GPIO4(+) | 63 | A_X1_GPIO16(+) |
| 24 | A_X1_GPIO4(-) | 64 | A_X1_GPIO16(-) |
| 25 | A_X1_GPIO5(+) | 65 | A_X1_GPIO17(+) |
| 26 | A_X1_GPIO5(-) | 66 | A_X1_GPIO17(-) |
| 27 | A_X1_GPIO6(+) | 67 | A_X1_GPIO18(+) |
| 28 | A_X1_GPIO6(-) | 68 | A_X1_GPIO18(-) |
| 29 | A_X1_GPIO7(+) | 69 | A_X1_GPIO19(+) |
| 30 | A_X1_GPIO7(-) | 70 | A_X1_GPIO19(-) |
| 31 | A_X1_GPIO8(+) | 71 | A_X1_GPIO20(+) |
| 32 | A_X1_GPIO8(-) | 72 | A_X1_GPIO20(-) |
| 33 | A_X1_GPIO9(+) | 73 | A_X1_GPIO21(+) |
| 34 | A_X1_GPIO9(-) | 74 | A_X1_GPIO21(-) |
| 35 | A_X1_GPIO10(+) | 75 | A_X1_GPIO22(+) |
| 36 | A_X1_GPIO10(-) | 76 | A_X1_GPIO22(-) |
| 37 | A_X1_GPIO11(+) | 77 | A_X1_GPIO23(+) |
| 38 | A_X1_GPIO11(-) | 78 | A_X1_GPIO23(-) |
| 39 | A_X1_GPIO12(+) | 79 | A_X1_GPIO24(+) |
| 40 | A_X1_GPIO12(-) | 80 | A_X1_GPIO24(-) |

Table 33. Flex-Circuit Connector “A_X1” Pin Assignment.

| Flex-Circuit Connector A_X2 <i>(connects module X2_TL, X2_BR, X2_TR or X2_BL)</i> | | | | |
|---|--------------|----------------|--------------|----------------|
| | <i>Pin #</i> | <i>Signal</i> | <i>Pin #</i> | <i>Signal</i> |
| | 1 | A_X2_GPIO12(-) | 41 | A_X2_GPIO24(-) |
| | 2 | A_X2_GPIO12(+) | 42 | A_X2_GPIO24(+) |
| | 3 | A_X2_GPIO11(-) | 43 | A_X2_GPIO23(-) |
| | 4 | A_X2_GPIO11(+) | 44 | A_X2_GPIO23(+) |
| | 5 | A_X2_GPIO10(-) | 45 | A_X2_GPIO22(-) |
| | 6 | A_X2_GPIO10(+) | 46 | A_X2_GPIO22(+) |
| | 7 | A_X2_GPIO9(-) | 47 | A_X2_GPIO21(-) |
| | 8 | A_X2_GPIO9(+) | 48 | A_X2_GPIO21(+) |
| | 9 | A_X2_GPIO8(-) | 49 | A_X2_GPIO20(-) |
| | 10 | A_X2_GPIO8(+) | 50 | A_X2_GPIO20(+) |
| | 11 | A_X2_GPIO7(-) | 51 | A_X2_GPIO19(-) |
| | 12 | A_X2_GPIO7(+) | 52 | A_X2_GPIO19(+) |
| | 13 | A_X2_GPIO6(-) | 53 | A_X2_GPIO18(-) |
| | 14 | A_X2_GPIO6(+) | 54 | A_X2_GPIO18(+) |
| | 15 | A_X2_GPIO5(-) | 55 | A_X2_GPIO17(-) |
| | 16 | A_X2_GPIO5(+) | 56 | A_X2_GPIO17(+) |
| | 17 | A_X2_GPIO4(-) | 57 | A_X2_GPIO16(-) |
| | 18 | A_X2_GPIO4(+) | 58 | A_X2_GPIO16(+) |
| | 19 | A_X2_GPIO3(-) | 59 | A_X2_GPIO15(-) |
| | 20 | A_X2_GPIO3(+) | 60 | A_X2_GPIO15(+) |
| | 21 | A_X2_GPIO2(-) | 61 | A_X2_GPIO14(-) |
| | 22 | A_X2_GPIO2(+) | 62 | A_X2_GPIO14(+) |
| | 23 | A_X2_GPIO1(-) | 63 | A_X2_GPIO13(-) |
| | 24 | A_X2_GPIO1(+) | 64 | A_X2_GPIO13(+) |
| | 25 | A_X2_DGND | 65 | A_X2_AGND |
| | 26 | A_X2_DGND | 66 | A_X2_AGND |
| | 27 | A_X2_DGND | 67 | A_X2_AGND |
| | 28 | A_X2_DSense(-) | 68 | A_X2_ASense(-) |
| | 29 | A_X2_DSense(+) | 69 | A_X2_ASense(+) |
| | 30 | A_X2_Vddd | 70 | A_X2_Vdda |
| | 31 | A_X2_Vddd | 71 | A_X2_Vdda |
| | 32 | A_X2_Vddd | 72 | A_X2_Vdda |
| | 33 | A_X2_DGND | 73 | A_X2_AGND |
| | 34 | *REMOVED* | 74 | A_X2_INJECT(-) |
| | 35 | *REMOVED* | 75 | A_X2_INJECT(+) |
| | 36 | *REMOVED* | 76 | *NO CONNECT* |
| | 37 | *REMOVED* | 77 | *NO CONNECT* |
| | 38 | *REMOVED* | 78 | *NO CONNECT* |
| | 39 | *REMOVED* | 79 | *NO CONNECT* |
| | 40 | A_X2_Vbias(+) | 80 | A_X2_Vbias(-) |

Table 34. Flex-Circuit Connector “A_X2” Pin Assignment.

| Flex-Circuit Connector A_X3 <i>(connects module X3_TL, X3_BR, X3_TR or X3_BL)</i> | | | |
|---|----------------|--------------|----------------|
| <i>Pin #</i> | <i>Signal</i> | <i>Pin #</i> | <i>Signal</i> |
| 1 | A_X3_Vbias(+) | 41 | A_X3_Vbias(-) |
| 2 | *REMOVED* | 42 | *NO CONNECT* |
| 3 | *REMOVED* | 43 | *NO CONNECT* |
| 4 | *REMOVED* | 44 | *NO CONNECT* |
| 5 | *REMOVED* | 45 | *NO CONNECT* |
| 6 | *REMOVED* | 46 | A_X3_INJECT(+) |
| 7 | *REMOVED* | 47 | A_X3_INJECT(-) |
| 8 | A_X3_DGND | 48 | A_X3_AGND |
| 9 | A_X3_Vddd | 49 | A_X3_Vdda |
| 10 | A_X3_Vddd | 50 | A_X3_Vdda |
| 11 | A_X3_Vddd | 51 | A_X3_Vdda |
| 12 | A_X3_DSense(+) | 52 | A_X3_ASense(+) |
| 13 | A_X3_DSense(-) | 53 | A_X3_ASense(-) |
| 14 | A_X3_DGND | 54 | A_X3_AGND |
| 15 | A_X3_DGND | 55 | A_X3_AGND |
| 16 | A_X3_DGND | 56 | A_X3_AGND |
| 17 | A_X3_GPIO1(+) | 57 | A_X3_GPIO13(+) |
| 18 | A_X3_GPIO1(-) | 58 | A_X3_GPIO13(-) |
| 19 | A_X3_GPIO2(+) | 59 | A_X3_GPIO14(+) |
| 20 | A_X3_GPIO2(-) | 60 | A_X3_GPIO14(-) |
| 21 | A_X3_GPIO3(+) | 61 | A_X3_GPIO15(+) |
| 22 | A_X3_GPIO3(-) | 62 | A_X3_GPIO15(-) |
| 23 | A_X3_GPIO4(+) | 63 | A_X3_GPIO16(+) |
| 24 | A_X3_GPIO4(-) | 64 | A_X3_GPIO16(-) |
| 25 | A_X3_GPIO5(+) | 65 | A_X3_GPIO17(+) |
| 26 | A_X3_GPIO5(-) | 66 | A_X3_GPIO17(-) |
| 27 | A_X3_GPIO6(+) | 67 | A_X3_GPIO18(+) |
| 28 | A_X3_GPIO6(-) | 68 | A_X3_GPIO18(-) |
| 29 | A_X3_GPIO7(+) | 69 | A_X3_GPIO19(+) |
| 30 | A_X3_GPIO7(-) | 70 | A_X3_GPIO19(-) |
| 31 | A_X3_GPIO8(+) | 71 | A_X3_GPIO20(+) |
| 32 | A_X3_GPIO8(-) | 72 | A_X3_GPIO20(-) |
| 33 | A_X3_GPIO9(+) | 73 | A_X3_GPIO21(+) |
| 34 | A_X3_GPIO9(-) | 74 | A_X3_GPIO21(-) |
| 35 | A_X3_GPIO10(+) | 75 | A_X3_GPIO22(+) |
| 36 | A_X3_GPIO10(-) | 76 | A_X3_GPIO22(-) |
| 37 | A_X3_GPIO11(+) | 77 | A_X3_GPIO23(+) |
| 38 | A_X3_GPIO11(-) | 78 | A_X3_GPIO23(-) |
| 39 | A_X3_GPIO12(+) | 79 | A_X3_GPIO24(+) |
| 40 | A_X3_GPIO12(-) | 80 | A_X3_GPIO24(-) |

Table 35. Flex-Circuit Connector “A_X3” Pin Assignment.

| Flex-Circuit Connector A_X4 <i>(connects module X4_TL, X4_BR, X4_TR or X4_BL)</i> | | | | |
|---|--------------|----------------|--------------|----------------|
| | <i>Pin #</i> | <i>Signal</i> | <i>Pin #</i> | <i>Signal</i> |
| | 1 | A_X4_GPIO12(-) | 41 | A_X4_GPIO24(-) |
| | 2 | A_X4_GPIO12(+) | 42 | A_X4_GPIO24(+) |
| | 3 | A_X4_GPIO11(-) | 43 | A_X4_GPIO23(-) |
| | 4 | A_X4_GPIO11(+) | 44 | A_X4_GPIO23(+) |
| | 5 | A_X4_GPIO10(-) | 45 | A_X4_GPIO22(-) |
| | 6 | A_X4_GPIO10(+) | 46 | A_X4_GPIO22(+) |
| | 7 | A_X4_GPIO9(-) | 47 | A_X4_GPIO21(-) |
| | 8 | A_X4_GPIO9(+) | 48 | A_X4_GPIO21(+) |
| | 9 | A_X4_GPIO8(-) | 49 | A_X4_GPIO20(-) |
| | 10 | A_X4_GPIO8(+) | 50 | A_X4_GPIO20(+) |
| | 11 | A_X4_GPIO7(-) | 51 | A_X4_GPIO19(-) |
| | 12 | A_X4_GPIO7(+) | 52 | A_X4_GPIO19(+) |
| | 13 | A_X4_GPIO6(-) | 53 | A_X4_GPIO18(-) |
| | 14 | A_X4_GPIO6(+) | 54 | A_X4_GPIO18(+) |
| | 15 | A_X4_GPIO5(-) | 55 | A_X4_GPIO17(-) |
| | 16 | A_X4_GPIO5(+) | 56 | A_X4_GPIO17(+) |
| | 17 | A_X4_GPIO4(-) | 57 | A_X4_GPIO16(-) |
| | 18 | A_X4_GPIO4(+) | 58 | A_X4_GPIO16(+) |
| | 19 | A_X4_GPIO3(-) | 59 | A_X4_GPIO15(-) |
| | 20 | A_X4_GPIO3(+) | 60 | A_X4_GPIO15(+) |
| | 21 | A_X4_GPIO2(-) | 61 | A_X4_GPIO14(-) |
| | 22 | A_X4_GPIO2(+) | 62 | A_X4_GPIO14(+) |
| | 23 | A_X4_GPIO1(-) | 63 | A_X4_GPIO13(-) |
| | 24 | A_X4_GPIO1(+) | 64 | A_X4_GPIO13(+) |
| | 25 | A_X4_DGND | 65 | A_X4_AGNND |
| | 26 | A_X4_DGND | 66 | A_X4_AGNND |
| | 27 | A_X4_DGND | 67 | A_X4_AGNND |
| | 28 | A_X4_DSense(-) | 68 | A_X4_ASense(-) |
| | 29 | A_X4_DSense(+) | 69 | A_X4_ASense(+) |
| | 30 | A_X4_Vddd | 70 | A_X4_Vdda |
| | 31 | A_X4_Vddd | 71 | A_X4_Vdda |
| | 32 | A_X4_Vddd | 72 | A_X4_Vdda |
| | 33 | A_X4_DGND | 73 | A_X4_AGNND |
| | 34 | *REMOVED* | 74 | A_X4_INJECT(-) |
| | 35 | *REMOVED* | 75 | A_X4_INJECT(+) |
| | 36 | *REMOVED* | 76 | *NO CONNECT* |
| | 37 | *REMOVED* | 77 | *NO CONNECT* |
| | 38 | *REMOVED* | 78 | *NO CONNECT* |
| | 39 | *REMOVED* | 79 | *NO CONNECT* |
| | 40 | A_X4_Vbias(+) | 80 | A_X4_Vbias(-) |

Table 36. Flex-Circuit Connector “A_X4” Pin Assignment.

| Flex-Circuit Connector A_X5 <i>(connects module X5_TL, X5_BR, X5_TR or X5_BL)</i> | | | | |
|---|--------------|----------------|--------------|----------------|
| | Pin # | Signal | Pin # | Signal |
| | 1 | A_X5_Vbias(+) | 41 | A_X5_Vbias(-) |
| | 2 | *REMOVED* | 42 | *NO CONNECT* |
| | 3 | *REMOVED* | 43 | *NO CONNECT* |
| | 4 | *REMOVED* | 44 | *NO CONNECT* |
| | 5 | *REMOVED* | 45 | *NO CONNECT* |
| | 6 | *REMOVED* | 46 | A_X5_INJECT(+) |
| | 7 | *REMOVED* | 47 | A_X5_INJECT(-) |
| | 8 | A_X5_DGND | 48 | A_X5_AGND |
| | 9 | A_X5_Vddd | 49 | A_X5_Vdda |
| | 10 | A_X5_Vddd | 50 | A_X5_Vdda |
| | 11 | A_X5_Vddd | 51 | A_X5_Vdda |
| | 12 | A_X5_DSense(+) | 52 | A_X5_ASense(+) |
| | 13 | A_X5_DSense(-) | 53 | A_X5_ASense(-) |
| | 14 | A_X5_DGND | 54 | A_X5_AGND |
| | 15 | A_X5_DGND | 55 | A_X5_AGND |
| | 16 | A_X5_DGND | 56 | A_X5_AGND |
| | 17 | A_X5_GPIO1(+) | 57 | A_X5_GPIO13(+) |
| | 18 | A_X5_GPIO1(-) | 58 | A_X5_GPIO13(-) |
| | 19 | A_X5_GPIO2(+) | 59 | A_X5_GPIO14(+) |
| | 20 | A_X5_GPIO2(-) | 60 | A_X5_GPIO14(-) |
| | 21 | A_X5_GPIO3(+) | 61 | A_X5_GPIO15(+) |
| | 22 | A_X5_GPIO3(-) | 62 | A_X5_GPIO15(-) |
| | 23 | A_X5_GPIO4(+) | 63 | A_X5_GPIO16(+) |
| | 24 | A_X5_GPIO4(-) | 64 | A_X5_GPIO16(-) |
| | 25 | A_X5_GPIO5(+) | 65 | A_X5_GPIO17(+) |
| | 26 | A_X5_GPIO5(-) | 66 | A_X5_GPIO17(-) |
| | 27 | A_X5_GPIO6(+) | 67 | A_X5_GPIO18(+) |
| | 28 | A_X5_GPIO6(-) | 68 | A_X5_GPIO18(-) |
| | 29 | A_X5_GPIO7(+) | 69 | A_X5_GPIO19(+) |
| | 30 | A_X5_GPIO7(-) | 70 | A_X5_GPIO19(-) |
| | 31 | A_X5_GPIO8(+) | 71 | A_X5_GPIO20(+) |
| | 32 | A_X5_GPIO8(-) | 72 | A_X5_GPIO20(-) |
| | 33 | A_X5_GPIO9(+) | 73 | A_X5_GPIO21(+) |
| | 34 | A_X5_GPIO9(-) | 74 | A_X5_GPIO21(-) |
| | 35 | A_X5_GPIO10(+) | 75 | A_X5_GPIO22(+) |
| | 36 | A_X5_GPIO10(-) | 76 | A_X5_GPIO22(-) |
| | 37 | A_X5_GPIO11(+) | 77 | A_X5_GPIO23(+) |
| | 38 | A_X5_GPIO11(-) | 78 | A_X5_GPIO23(-) |
| | 39 | A_X5_GPIO12(+) | 79 | A_X5_GPIO24(+) |
| | 40 | A_X5_GPIO12(-) | 80 | A_X5_GPIO24(-) |

Table 37. Flex-Circuit Connector “A_X5” Pin Assignment.

| Flex-Circuit Connector A_X6 <i>(connects module X6_TL or X6_BR)</i> | | | | |
|---|--------------|----------------|--------------|----------------|
| | Pin # | Signal | Pin # | Signal |
| | 1 | A_X4_GPIO12(-) | 41 | A_X4_GPIO24(-) |
| | 2 | A_X4_GPIO12(+) | 42 | A_X4_GPIO24(+) |
| | 3 | A_X4_GPIO11(-) | 43 | A_X4_GPIO23(-) |
| | 4 | A_X4_GPIO11(+) | 44 | A_X4_GPIO23(+) |
| | 5 | A_X4_GPIO10(-) | 45 | A_X4_GPIO22(-) |
| | 6 | A_X4_GPIO10(+) | 46 | A_X4_GPIO22(+) |
| | 7 | A_X4_GPIO9(-) | 47 | A_X4_GPIO21(-) |
| | 8 | A_X4_GPIO9(+) | 48 | A_X4_GPIO21(+) |
| | 9 | A_X4_GPIO8(-) | 49 | A_X4_GPIO20(-) |
| | 10 | A_X4_GPIO8(+) | 50 | A_X4_GPIO20(+) |
| | 11 | A_X4_GPIO7(-) | 51 | A_X4_GPIO19(-) |
| | 12 | A_X4_GPIO7(+) | 52 | A_X4_GPIO19(+) |
| | 13 | A_X4_GPIO6(-) | 53 | A_X4_GPIO18(-) |
| | 14 | A_X4_GPIO6(+) | 54 | A_X4_GPIO18(+) |
| | 15 | A_X4_GPIO5(-) | 55 | A_X4_GPIO17(-) |
| | 16 | A_X4_GPIO5(+) | 56 | A_X4_GPIO17(+) |
| | 17 | A_X4_GPIO4(-) | 57 | A_X4_GPIO16(-) |
| | 18 | A_X4_GPIO4(+) | 58 | A_X4_GPIO16(+) |
| | 19 | A_X4_GPIO3(-) | 59 | A_X4_GPIO15(-) |
| | 20 | A_X4_GPIO3(+) | 60 | A_X4_GPIO15(+) |
| | 21 | A_X4_GPIO2(-) | 61 | A_X4_GPIO14(-) |
| | 22 | A_X4_GPIO2(+) | 62 | A_X4_GPIO14(+) |
| | 23 | A_X4_GPIO1(-) | 63 | A_X4_GPIO13(-) |
| | 24 | A_X4_GPIO1(+) | 64 | A_X4_GPIO13(+) |
| | 25 | A_X4_DGND | 65 | A_X4_AGND |
| | 26 | A_X4_DGND | 66 | A_X4_AGND |
| | 27 | A_X4_DGND | 67 | A_X4_AGND |
| | 28 | A_X4_DSense(-) | 68 | A_X4_ASense(-) |
| | 29 | A_X4_DSense(+) | 69 | A_X4_ASense(+) |
| | 30 | A_X4_Vddd | 70 | A_X4_Vdda |
| | 31 | A_X4_Vddd | 71 | A_X4_Vdda |
| | 32 | A_X4_Vddd | 72 | A_X4_Vdda |
| | 33 | A_X4_DGND | 73 | A_X4_AGND |
| | 34 | *REMOVED* | 74 | A_X4_INJECT(-) |
| | 35 | *REMOVED* | 75 | A_X4_INJECT(+) |
| | 36 | *REMOVED* | 76 | *NO CONNECT* |
| | 37 | *REMOVED* | 77 | *NO CONNECT* |
| | 38 | *REMOVED* | 78 | *NO CONNECT* |
| | 39 | *REMOVED* | 79 | *NO CONNECT* |
| | 40 | A_X4_Vbias(+) | 80 | A_X4_Vbias(-) |

Table 38. Flex-Circuit Connector “A_X6” Pin Assignment.

| Flex-Circuit Connector A_X7 <i>(connects module X7_TL or X7_BR)</i> | | | | |
|---|--------------|------------------|--------------|------------------|
| | Pin # | Signal | Pin # | Signal |
| | 1 | A_X7Y9_Vbias(+) | 41 | A_X7Y9_Vbias(-) |
| | 2 | *REMOVED* | 42 | *NO CONNECT* |
| | 3 | *REMOVED* | 43 | *NO CONNECT* |
| | 4 | *REMOVED* | 44 | *NO CONNECT* |
| | 5 | *REMOVED* | 45 | *NO CONNECT* |
| | 6 | *REMOVED* | 46 | A_X7Y9_INJECT(+) |
| | 7 | *REMOVED* | 47 | A_X7Y9_INJECT(-) |
| | 8 | A_X7Y9_DGND | 48 | A_X7Y9_AGND |
| | 9 | A_X7Y9_Vddd | 49 | A_X7Y9_Vdda |
| | 10 | A_X7Y9_Vddd | 50 | A_X7Y9_Vdda |
| | 11 | A_X7Y9_Vddd | 51 | A_X7Y9_Vdda |
| | 12 | A_X7Y9_DSense(+) | 52 | A_X7Y9_ASense(+) |
| | 13 | A_X7Y9_DSense(-) | 53 | A_X7Y9_ASense(-) |
| | 14 | A_X7Y9_DGND | 54 | A_X7Y9_AGND |
| | 15 | A_X7Y9_DGND | 55 | A_X7Y9_AGND |
| | 16 | A_X7Y9_DGND | 56 | A_X7Y9_AGND |
| | 17 | A_X7Y9_GPIO1(+) | 57 | A_X7Y9_GPIO13(+) |
| | 18 | A_X7Y9_GPIO1(-) | 58 | A_X7Y9_GPIO13(-) |
| | 19 | A_X7Y9_GPIO2(+) | 59 | A_X7Y9_GPIO14(+) |
| | 20 | A_X7Y9_GPIO2(-) | 60 | A_X7Y9_GPIO14(-) |
| | 21 | A_X7Y9_GPIO3(+) | 61 | A_X7Y9_GPIO15(+) |
| | 22 | A_X7Y9_GPIO3(-) | 62 | A_X7Y9_GPIO15(-) |
| | 23 | A_X7Y9_GPIO4(+) | 63 | A_X7Y9_GPIO16(+) |
| | 24 | A_X7Y9_GPIO4(-) | 64 | A_X7Y9_GPIO16(-) |
| | 25 | A_X7Y9_GPIO5(+) | 65 | A_X7Y9_GPIO17(+) |
| | 26 | A_X7Y9_GPIO5(-) | 66 | A_X7Y9_GPIO17(-) |
| | 27 | A_X7Y9_GPIO6(+) | 67 | A_X7Y9_GPIO18(+) |
| | 28 | A_X7Y9_GPIO6(-) | 68 | A_X7Y9_GPIO18(-) |
| | 29 | A_X7Y9_GPIO7(+) | 69 | A_X7Y9_GPIO19(+) |
| | 30 | A_X7Y9_GPIO7(-) | 70 | A_X7Y9_GPIO19(-) |
| | 31 | A_X7Y9_GPIO8(+) | 71 | A_X7Y9_GPIO20(+) |
| | 32 | A_X7Y9_GPIO8(-) | 72 | A_X7Y9_GPIO20(-) |
| | 33 | A_X7Y9_GPIO9(+) | 73 | A_X7Y9_GPIO21(+) |
| | 34 | A_X7Y9_GPIO9(-) | 74 | A_X7Y9_GPIO21(-) |
| | 35 | A_X7Y9_GPIO10(+) | 75 | A_X7Y9_GPIO22(+) |
| | 36 | A_X7Y9_GPIO10(-) | 76 | A_X7Y9_GPIO22(-) |
| | 37 | A_X7Y9_GPIO11(+) | 77 | A_X7Y9_GPIO23(+) |
| | 38 | A_X7Y9_GPIO11(-) | 78 | A_X7Y9_GPIO23(-) |
| | 39 | A_X7Y9_GPIO12(+) | 79 | A_X7Y9_GPIO24(+) |
| | 40 | A_X7Y9_GPIO12(-) | 80 | A_X7Y9_GPIO24(-) |

Table 39. Flex-Circuit Connector “A_X7” Pin Assignment.

| <i>Flex-Circuit Connector A_Y1</i> <i>(connects module Y1_TL, Y1_BR, Y1_TR or Y1_BL)</i> | | | | | | |
|---|--------------|----------------|------------|--------------|----------------|------------|
| | <i>Pin #</i> | <i>Signal</i> | <i>I/O</i> | <i>Pin #</i> | <i>Signal</i> | <i>I/O</i> |
| | 1 | A_Y1_Vbias(+) | | 51 | A_Y1_Vbias(-) | |
| | 2 | *REMOVED* | | 52 | *NO CONNECT* | |
| | 3 | *REMOVED* | | 53 | *NO CONNECT* | |
| | 4 | *REMOVED* | | 54 | *NO CONNECT* | |
| | 5 | *REMOVED* | | 55 | *NO CONNECT* | |
| | 6 | *REMOVED* | | 56 | A_Y1_INJECT(+) | |
| | 7 | *REMOVED* | | 57 | A_Y1_INJECT(-) | |
| | 8 | A_Y1_DGND | | 58 | A_Y1_AGND | |
| | 9 | A_Y1_Vddd | | 59 | A_Y1_Vdda | |
| | 10 | A_Y1_Vddd | | 60 | A_Y1_Vdda | |
| | 11 | A_Y1_Vddd | | 61 | A_Y1_Vdda | |
| | 12 | A_Y1_DSense(+) | | 62 | A_Y1_ASense(+) | |
| | 13 | A_Y1_DSense(-) | | 63 | A_Y1_ASense(-) | |
| | 14 | A_Y1_DGND | | 64 | A_Y1_AGND | |
| | 15 | A_Y1_DGND | | 65 | A_Y1_AGND | |
| | 16 | A_Y1_DGND | | 66 | A_Y1_AGND | |
| | 17 | A_Y1_GPIO1(+) | | 67 | A_Y1_GPIO18(+) | |
| | 18 | A_Y1_GPIO1(-) | | 68 | A_Y1_GPIO18(-) | |
| | 19 | A_Y1_GPIO2(+) | | 69 | A_Y1_GPIO19(+) | |
| | 20 | A_Y1_GPIO2(-) | | 70 | A_Y1_GPIO19(-) | |
| | 21 | A_Y1_GPIO3(+) | | 71 | A_Y1_GPIO20(+) | |
| | 22 | A_Y1_GPIO3(-) | | 72 | A_Y1_GPIO20(-) | |
| | 23 | A_Y1_GPIO4(+) | | 73 | A_Y1_GPIO21(+) | |
| | 24 | A_Y1_GPIO4(-) | | 74 | A_Y1_GPIO21(-) | |
| | 25 | A_Y1_GPIO5(+) | | 75 | A_Y1_GPIO22(+) | |
| | 26 | A_Y1_GPIO5(-) | | 76 | A_Y1_GPIO22(-) | |
| | 27 | A_Y1_GPIO6(+) | | 77 | A_Y1_GPIO23(+) | |
| | 28 | A_Y1_GPIO6(-) | | 78 | A_Y1_GPIO23(-) | |
| | 29 | A_Y1_GPIO7(+) | | 79 | A_Y1_GPIO24(+) | |
| | 30 | A_Y1_GPIO7(-) | | 80 | A_Y1_GPIO24(-) | |
| | 31 | A_Y1_GPIO8(+) | | 81 | A_Y1_GPIO25(+) | |
| | 32 | A_Y1_GPIO8(-) | | 82 | A_Y1_GPIO25(-) | |
| | 33 | A_Y1_GPIO9(+) | | 83 | A_Y1_GPIO26(+) | |
| | 34 | A_Y1_GPIO9(-) | | 84 | A_Y1_GPIO26(-) | |
| | 35 | A_Y1_GPIO10(+) | | 85 | A_Y1_GPIO27(+) | |
| | 36 | A_Y1_GPIO10(-) | | 86 | A_Y1_GPIO27(-) | |
| | 37 | A_Y1_GPIO11(+) | | 87 | A_Y1_GPIO28(+) | |
| | 38 | A_Y1_GPIO11(-) | | 88 | A_Y1_GPIO28(-) | |
| | 39 | A_Y1_GPIO12(+) | | 89 | A_Y1_GPIO29(+) | |
| | 40 | A_Y1_GPIO12(-) | | 90 | A_Y1_GPIO29(-) | |
| | 41 | A_Y1_GPIO13(+) | | 91 | A_Y1_GPIO30(+) | |
| | 42 | A_Y1_GPIO13(-) | | 92 | A_Y1_GPIO30(-) | |
| | 43 | A_Y1_GPIO14(+) | | 93 | A_Y1_GPIO31(+) | |
| | 44 | A_Y1_GPIO14(-) | | 94 | A_Y1_GPIO31(-) | |
| | 45 | A_Y1_GPIO15(+) | | 95 | A_Y1_GPIO32(+) | |
| | 46 | A_Y1_GPIO15(-) | | 96 | A_Y1_GPIO32(-) | |
| | 47 | A_Y1_GPIO16(+) | | 97 | A_Y1_GPIO33(+) | |
| | 48 | A_Y1_GPIO16(-) | | 98 | A_Y1_GPIO33(-) | |
| | 49 | A_Y1_GPIO17(+) | | 99 | A_Y1_GPIO34(+) | |
| | 50 | A_Y1_GPIO17(-) | | 100 | A_Y1_GPIO34(-) | |

Table 40. Flex-Circuit Connector “A_Y1” Pin Assignment.

| Flex-Circuit Connector A_Y2 <i>(connects module Y2_TL, Y2_BR, Y2_TR or Y2_BL)</i> | | | | |
|---|--------------|----------------|--------------|----------------|
| | Pin # | Signal | Pin # | Signal |
| | 1 | *NO CONNECT* | 51 | *NO CONNECT* |
| | 2 | *NO CONNECT* | 52 | *NO CONNECT* |
| | 3 | *NO CONNECT* | 53 | *NO CONNECT* |
| | 4 | *NO CONNECT* | 54 | *NO CONNECT* |
| | 5 | A_Y2_GPIO15(-) | 55 | A_Y2_GPIO30(-) |
| | 6 | A_Y2_GPIO15(+) | 56 | A_Y2_GPIO30(+) |
| | 7 | A_Y2_GPIO14(-) | 57 | A_Y2_GPIO29(-) |
| | 8 | A_Y2_GPIO14(+) | 58 | A_Y2_GPIO29(+) |
| | 9 | A_Y2_GPIO13(-) | 59 | A_Y2_GPIO28(-) |
| | 10 | A_Y2_GPIO13(+) | 60 | A_Y2_GPIO28(+) |
| | 11 | A_Y2_GPIO12(-) | 61 | A_Y2_GPIO27(-) |
| | 12 | A_Y2_GPIO12(+) | 62 | A_Y2_GPIO27(+) |
| | 13 | A_Y2_GPIO11(-) | 63 | A_Y2_GPIO26(-) |
| | 14 | A_Y2_GPIO11(+) | 64 | A_Y2_GPIO26(+) |
| | 15 | A_Y2_GPIO10(-) | 65 | A_Y2_GPIO25(-) |
| | 16 | A_Y2_GPIO10(+) | 66 | A_Y2_GPIO25(+) |
| | 17 | A_Y2_GPIO9(-) | 67 | A_Y2_GPIO24(-) |
| | 18 | A_Y2_GPIO9(+) | 68 | A_Y2_GPIO24(+) |
| | 19 | A_Y2_GPIO8(-) | 69 | A_Y2_GPIO23(-) |
| | 20 | A_Y2_GPIO8(+) | 70 | A_Y2_GPIO23(+) |
| | 21 | A_Y2_GPIO7(-) | 71 | A_Y2_GPIO22(-) |
| | 22 | A_Y2_GPIO7(+) | 72 | A_Y2_GPIO22(+) |
| | 23 | A_Y2_GPIO6(-) | 73 | A_Y2_GPIO21(-) |
| | 24 | A_Y2_GPIO6(+) | 74 | A_Y2_GPIO21(+) |
| | 25 | A_Y2_GPIO5(-) | 75 | A_Y2_GPIO20(-) |
| | 26 | A_Y2_GPIO5(+) | 76 | A_Y2_GPIO20(+) |
| | 27 | A_Y2_GPIO4(-) | 77 | A_Y2_GPIO19(-) |
| | 28 | A_Y2_GPIO4(+) | 78 | A_Y2_GPIO19(+) |
| | 29 | A_Y2_GPIO3(-) | 79 | A_Y2_GPIO18(-) |
| | 30 | A_Y2_GPIO3(+) | 80 | A_Y2_GPIO18(+) |
| | 31 | A_Y2_GPIO2(-) | 81 | A_Y2_GPIO17(-) |
| | 32 | A_Y2_GPIO2(+) | 82 | A_Y2_GPIO17(+) |
| | 33 | A_Y2_GPIO1(-) | 83 | A_Y2_GPIO16(-) |
| | 34 | A_Y2_GPIO1(+) | 84 | A_Y2_GPIO16(+) |
| | 35 | A_Y2_DGND | 85 | A_Y2_AGND |
| | 36 | A_Y2_DGND | 86 | A_Y2_AGND |
| | 37 | A_Y2_DGND | 87 | A_Y2_AGND |
| | 38 | A_Y2_DSense(-) | 88 | A_Y2_ASense(-) |
| | 39 | A_Y2_DSense(+) | 89 | A_Y2_ASense(+) |
| | 40 | A_Y2_Vddd | 90 | A_Y2_Vdda |
| | 41 | A_Y2_Vddd | 91 | A_Y2_Vdda |
| | 42 | A_Y2_Vddd | 92 | A_Y2_Vdda |
| | 43 | A_Y2_DGND | 93 | A_Y2_AGND |
| | 44 | *REMOVED* | 94 | A_Y2_INJECT(-) |
| | 45 | *REMOVED* | 95 | A_Y2_INJECT(+) |
| | 46 | *REMOVED* | 96 | *NO CONNECT* |
| | 47 | *REMOVED* | 97 | *NO CONNECT* |
| | 48 | *REMOVED* | 98 | *NO CONNECT* |
| | 49 | *REMOVED* | 99 | *NO CONNECT* |
| | 50 | A_Y2_Vbias(+) | 100 | A_Y2_Vbias(-) |

Table 41. Flex-Circuit Connector “A_Y2” Pin Assignment.

| Flex-Circuit Connector A_Y3 (connects module Y3_TL, Y3_BR, Y3_TR or Y3_BL) | | | | | | |
|---|-------|----------------|-----|-------|----------------|-----|
| | Pin # | Signal | I/O | Pin # | Signal | I/O |
| | 1 | A_Y3_Vbias(+) | | 51 | A_Y3_Vbias(-) | |
| | 2 | *REMOVED* | | 52 | *NO CONNECT* | |
| | 3 | *REMOVED* | | 53 | *NO CONNECT* | |
| | 4 | *REMOVED* | | 54 | *NO CONNECT* | |
| | 5 | *REMOVED* | | 55 | *NO CONNECT* | |
| | 6 | *REMOVED* | | 56 | A_Y3_INJECT(+) | |
| | 7 | *REMOVED* | | 57 | A_Y3_INJECT(-) | |
| | 8 | A_Y3_DGND | | 58 | A_Y3_AGND | |
| | 9 | A_Y3_Vddd | | 59 | A_Y3_Vdda | |
| | 10 | A_Y3_Vddd | | 60 | A_Y3_Vdda | |
| | 11 | A_Y3_Vddd | | 61 | A_Y3_Vdda | |
| | 12 | A_Y3_DSense(+) | | 62 | A_Y3_ASense(+) | |
| | 13 | A_Y3_DSense(-) | | 63 | A_Y3_ASense(-) | |
| | 14 | A_Y3_DGND | | 64 | A_Y3_AGND | |
| | 15 | A_Y3_DGND | | 65 | A_Y3_AGND | |
| | 16 | A_Y3_DGND | | 66 | A_Y3_AGND | |
| | 17 | A_Y3_GPIO1(+) | | 67 | A_Y3_GPIO16(+) | |
| | 18 | A_Y3_GPIO1(-) | | 68 | A_Y3_GPIO16(-) | |
| | 19 | A_Y3_GPIO2(+) | | 69 | A_Y3_GPIO17(+) | |
| | 20 | A_Y3_GPIO2(-) | | 70 | A_Y3_GPIO17(-) | |
| | 21 | A_Y3_GPIO3(+) | | 71 | A_Y3_GPIO18(+) | |
| | 22 | A_Y3_GPIO3(-) | | 72 | A_Y3_GPIO18(-) | |
| | 23 | A_Y3_GPIO4(+) | | 73 | A_Y3_GPIO19(+) | |
| | 24 | A_Y3_GPIO4(-) | | 74 | A_Y3_GPIO19(-) | |
| | 25 | A_Y3_GPIO5(+) | | 75 | A_Y3_GPIO20(+) | |
| | 26 | A_Y3_GPIO5(-) | | 76 | A_Y3_GPIO20(-) | |
| | 27 | A_Y3_GPIO6(+) | | 77 | A_Y3_GPIO21(+) | |
| | 28 | A_Y3_GPIO6(-) | | 78 | A_Y3_GPIO21(-) | |
| | 29 | A_Y3_GPIO7(+) | | 79 | A_Y3_GPIO22(+) | |
| | 30 | A_Y3_GPIO7(-) | | 80 | A_Y3_GPIO22(-) | |
| | 31 | A_Y3_GPIO8(+) | | 81 | A_Y3_GPIO23(+) | |
| | 32 | A_Y3_GPIO8(-) | | 82 | A_Y3_GPIO23(-) | |
| | 33 | A_Y3_GPIO9(+) | | 83 | A_Y3_GPIO24(+) | |
| | 34 | A_Y3_GPIO9(-) | | 84 | A_Y3_GPIO24(-) | |
| | 35 | A_Y3_GPIO10(+) | | 85 | A_Y3_GPIO25(+) | |
| | 36 | A_Y3_GPIO10(-) | | 86 | A_Y3_GPIO25(-) | |
| | 37 | A_Y3_GPIO11(+) | | 87 | A_Y3_GPIO26(+) | |
| | 38 | A_Y3_GPIO11(-) | | 88 | A_Y3_GPIO26(-) | |
| | 39 | A_Y3_GPIO12(+) | | 89 | A_Y3_GPIO27(+) | |
| | 40 | A_Y3_GPIO12(-) | | 90 | A_Y3_GPIO27(-) | |
| | 41 | A_Y3_GPIO13(+) | | 91 | A_Y3_GPIO28(+) | |
| | 42 | A_Y3_GPIO13(-) | | 92 | A_Y3_GPIO28(-) | |
| | 43 | A_Y3_GPIO14(+) | | 93 | A_Y3_GPIO29(+) | |
| | 44 | A_Y3_GPIO14(-) | | 94 | A_Y3_GPIO29(-) | |
| | 45 | A_Y3_GPIO15(+) | | 95 | A_Y3_GPIO30(+) | |
| | 46 | A_Y3_GPIO15(-) | | 96 | A_Y3_GPIO30(-) | |
| | 47 | *NO CONNECT* | | 97 | *NO CONNECT* | |
| | 48 | *NO CONNECT* | | 98 | *NO CONNECT* | |
| | 49 | *NO CONNECT* | | 99 | *NO CONNECT* | |
| | 50 | *NO CONNECT* | | 100 | *NO CONNECT* | |

Table 42. Flex-Circuit Connector “A_Y3” Pin Assignment.

| Flex-Circuit Connector A_Y4 <i>(connects module Y4_TL, Y4_BR, Y4_TR or Y4_BL)</i> | | | | |
|---|--------------|----------------|--------------|----------------|
| | <i>Pin #</i> | <i>Signal</i> | <i>Pin #</i> | <i>Signal</i> |
| | 1 | A_Y4_GPIO12(-) | 41 | A_Y4_GPIO24(-) |
| | 2 | A_Y4_GPIO12(+) | 42 | A_Y4_GPIO24(+) |
| | 3 | A_Y4_GPIO11(-) | 43 | A_Y4_GPIO23(-) |
| | 4 | A_Y4_GPIO11(+) | 44 | A_Y4_GPIO23(+) |
| | 5 | A_Y4_GPIO10(-) | 45 | A_Y4_GPIO22(-) |
| | 6 | A_Y4_GPIO10(+) | 46 | A_Y4_GPIO22(+) |
| | 7 | A_Y4_GPIO9(-) | 47 | A_Y4_GPIO21(-) |
| | 8 | A_Y4_GPIO9(+) | 48 | A_Y4_GPIO21(+) |
| | 9 | A_Y4_GPIO8(-) | 49 | A_Y4_GPIO20(-) |
| | 10 | A_Y4_GPIO8(+) | 50 | A_Y4_GPIO20(+) |
| | 11 | A_Y4_GPIO7(-) | 51 | A_Y4_GPIO19(-) |
| | 12 | A_Y4_GPIO7(+) | 52 | A_Y4_GPIO19(+) |
| | 13 | A_Y4_GPIO6(-) | 53 | A_Y4_GPIO18(-) |
| | 14 | A_Y4_GPIO6(+) | 54 | A_Y4_GPIO18(+) |
| | 15 | A_Y4_GPIO5(-) | 55 | A_Y4_GPIO17(-) |
| | 16 | A_Y4_GPIO5(+) | 56 | A_Y4_GPIO17(+) |
| | 17 | A_Y4_GPIO4(-) | 57 | A_Y4_GPIO16(-) |
| | 18 | A_Y4_GPIO4(+) | 58 | A_Y4_GPIO16(+) |
| | 19 | A_Y4_GPIO3(-) | 59 | A_Y4_GPIO15(-) |
| | 20 | A_Y4_GPIO3(+) | 60 | A_Y4_GPIO15(+) |
| | 21 | A_Y4_GPIO2(-) | 61 | A_Y4_GPIO14(-) |
| | 22 | A_Y4_GPIO2(+) | 62 | A_Y4_GPIO14(+) |
| | 23 | A_Y4_GPIO1(-) | 63 | A_Y4_GPIO13(-) |
| | 24 | A_Y4_GPIO1(+) | 64 | A_Y4_GPIO13(+) |
| | 25 | A_Y4_DGND | 65 | A_Y4_AGND |
| | 26 | A_Y4_DGND | 66 | A_Y4_AGND |
| | 27 | A_Y4_DGND | 67 | A_Y4_AGND |
| | 28 | A_Y4_DSense(-) | 68 | A_Y4_ASense(-) |
| | 29 | A_Y4_DSense(+) | 69 | A_Y4_ASense(+) |
| | 30 | A_Y4_Vddd | 70 | A_Y4_Vdda |
| | 31 | A_Y4_Vddd | 71 | A_Y4_Vdda |
| | 32 | A_Y4_Vddd | 72 | A_Y4_Vdda |
| | 33 | A_Y4_DGND | 73 | A_Y4_AGND |
| | 34 | *REMOVED* | 74 | A_Y4_INJECT(-) |
| | 35 | *REMOVED* | 75 | A_Y4_INJECT(+) |
| | 36 | *REMOVED* | 76 | *NO CONNECT* |
| | 37 | *REMOVED* | 77 | *NO CONNECT* |
| | 38 | *REMOVED* | 78 | *NO CONNECT* |
| | 39 | *REMOVED* | 79 | *NO CONNECT* |
| | 40 | A_Y4_Vbias(+) | 80 | A_Y4_Vbias(-) |

Table 43. Flex-Circuit Connector “A_Y4” Pin Assignment.

| Flex-Circuit Connector A_Y5 <i>(connects module Y5_TL, Y5_BR, Y5_TR or Y5_BL)</i> | | | | |
|---|--------------|----------------|--------------|----------------|
| | Pin # | Signal | Pin # | Signal |
| | 1 | A_Y5_Vbias(+) | 41 | A_Y5_Vbias(-) |
| | 2 | *REMOVED* | 42 | *NO CONNECT* |
| | 3 | *REMOVED* | 43 | *NO CONNECT* |
| | 4 | *REMOVED* | 44 | *NO CONNECT* |
| | 5 | *REMOVED* | 45 | *NO CONNECT* |
| | 6 | *REMOVED* | 46 | A_Y5_INJECT(+) |
| | 7 | *REMOVED* | 47 | A_Y5_INJECT(-) |
| | 8 | A_Y5_DGND | 48 | A_Y5_AGND |
| | 9 | A_Y5_Vddd | 49 | A_Y5_Vdda |
| | 10 | A_Y5_Vddd | 50 | A_Y5_Vdda |
| | 11 | A_Y5_Vddd | 51 | A_Y5_Vdda |
| | 12 | A_Y5_DSense(+) | 52 | A_Y5_ASense(+) |
| | 13 | A_Y5_DSense(-) | 53 | A_Y5_ASense(-) |
| | 14 | A_Y5_DGND | 54 | A_Y5_AGND |
| | 15 | A_Y5_DGND | 55 | A_Y5_AGND |
| | 16 | A_Y5_DGND | 56 | A_Y5_AGND |
| | 17 | A_Y5_GPIO1(+) | 57 | A_Y5_GPIO13(+) |
| | 18 | A_Y5_GPIO1(-) | 58 | A_Y5_GPIO13(-) |
| | 19 | A_Y5_GPIO2(+) | 59 | A_Y5_GPIO14(+) |
| | 20 | A_Y5_GPIO2(-) | 60 | A_Y5_GPIO14(-) |
| | 21 | A_Y5_GPIO3(+) | 61 | A_Y5_GPIO15(+) |
| | 22 | A_Y5_GPIO3(-) | 62 | A_Y5_GPIO15(-) |
| | 23 | A_Y5_GPIO4(+) | 63 | A_Y5_GPIO16(+) |
| | 24 | A_Y5_GPIO4(-) | 64 | A_Y5_GPIO16(-) |
| | 25 | A_Y5_GPIO5(+) | 65 | A_Y5_GPIO17(+) |
| | 26 | A_Y5_GPIO5(-) | 66 | A_Y5_GPIO17(-) |
| | 27 | A_Y5_GPIO6(+) | 67 | A_Y5_GPIO18(+) |
| | 28 | A_Y5_GPIO6(-) | 68 | A_Y5_GPIO18(-) |
| | 29 | A_Y5_GPIO7(+) | 69 | A_Y5_GPIO19(+) |
| | 30 | A_Y5_GPIO7(-) | 70 | A_Y5_GPIO19(-) |
| | 31 | A_Y5_GPIO8(+) | 71 | A_Y5_GPIO20(+) |
| | 32 | A_Y5_GPIO8(-) | 72 | A_Y5_GPIO20(-) |
| | 33 | A_Y5_GPIO9(+) | 73 | A_Y5_GPIO21(+) |
| | 34 | A_Y5_GPIO9(-) | 74 | A_Y5_GPIO21(-) |
| | 35 | A_Y5_GPIO10(+) | 75 | A_Y5_GPIO22(+) |
| | 36 | A_Y5_GPIO10(-) | 76 | A_Y5_GPIO22(-) |
| | 37 | A_Y5_GPIO11(+) | 77 | A_Y5_GPIO23(+) |
| | 38 | A_Y5_GPIO11(-) | 78 | A_Y5_GPIO23(-) |
| | 39 | A_Y5_GPIO12(+) | 79 | A_Y5_GPIO24(+) |
| | 40 | A_Y5_GPIO12(-) | 80 | A_Y5_GPIO24(-) |

Table 44. Flex-Circuit Connector “A_Y5” Pin Assignment.

| Flex-Circuit Connector A_Y6 <i>(connects module Y6_TL, Y6_BR, Y6_TR or Y6_BL)</i> | | | | |
|---|--------------|----------------|--------------|----------------|
| | Pin # | Signal | Pin # | Signal |
| | 1 | A_Y6_GPIO12(-) | 41 | A_Y6_GPIO24(-) |
| | 2 | A_Y6_GPIO12(+) | 42 | A_Y6_GPIO24(+) |
| | 3 | A_Y6_GPIO11(-) | 43 | A_Y6_GPIO23(-) |
| | 4 | A_Y6_GPIO11(+) | 44 | A_Y6_GPIO23(+) |
| | 5 | A_Y6_GPIO10(-) | 45 | A_Y6_GPIO22(-) |
| | 6 | A_Y6_GPIO10(+) | 46 | A_Y6_GPIO22(+) |
| | 7 | A_Y6_GPIO9(-) | 47 | A_Y6_GPIO21(-) |
| | 8 | A_Y6_GPIO9(+) | 48 | A_Y6_GPIO21(+) |
| | 9 | A_Y6_GPIO8(-) | 49 | A_Y6_GPIO20(-) |
| | 10 | A_Y6_GPIO8(+) | 50 | A_Y6_GPIO20(+) |
| | 11 | A_Y6_GPIO7(-) | 51 | A_Y6_GPIO19(-) |
| | 12 | A_Y6_GPIO7(+) | 52 | A_Y6_GPIO19(+) |
| | 13 | A_Y6_GPIO6(-) | 53 | A_Y6_GPIO18(-) |
| | 14 | A_Y6_GPIO6(+) | 54 | A_Y6_GPIO18(+) |
| | 15 | A_Y6_GPIO5(-) | 55 | A_Y6_GPIO17(-) |
| | 16 | A_Y6_GPIO5(+) | 56 | A_Y6_GPIO17(+) |
| | 17 | A_Y6_GPIO4(-) | 57 | A_Y6_GPIO16(-) |
| | 18 | A_Y6_GPIO4(+) | 58 | A_Y6_GPIO16(+) |
| | 19 | A_Y6_GPIO3(-) | 59 | A_Y6_GPIO15(-) |
| | 20 | A_Y6_GPIO3(+) | 60 | A_Y6_GPIO15(+) |
| | 21 | A_Y6_GPIO2(-) | 61 | A_Y6_GPIO14(-) |
| | 22 | A_Y6_GPIO2(+) | 62 | A_Y6_GPIO14(+) |
| | 23 | A_Y6_GPIO1(-) | 63 | A_Y6_GPIO13(-) |
| | 24 | A_Y6_GPIO1(+) | 64 | A_Y6_GPIO13(+) |
| | 25 | A_Y6_DGND | 65 | A_Y6_AGND |
| | 26 | A_Y6_DGND | 66 | A_Y6_AGND |
| | 27 | A_Y6_DGND | 67 | A_Y6_AGND |
| | 28 | A_Y6_DSense(-) | 68 | A_Y6_ASense(-) |
| | 29 | A_Y6_DSense(+) | 69 | A_Y6_ASense(+) |
| | 30 | A_Y6_Vddd | 70 | A_Y6_Vdda |
| | 31 | A_Y6_Vddd | 71 | A_Y6_Vdda |
| | 32 | A_Y6_Vddd | 72 | A_Y6_Vdda |
| | 33 | A_Y6_DGND | 73 | A_Y6_AGND |
| | 34 | *REMOVED* | 74 | A_Y6_INJECT(-) |
| | 35 | *REMOVED* | 75 | A_Y6_INJECT(+) |
| | 36 | *REMOVED* | 76 | *NO CONNECT* |
| | 37 | *REMOVED* | 77 | *NO CONNECT* |
| | 38 | *REMOVED* | 78 | *NO CONNECT* |
| | 39 | *REMOVED* | 79 | *NO CONNECT* |
| | 40 | A_Y6_Vbias(+) | 80 | A_Y6_Vbias(-) |

Table 45. Flex-Circuit Connector “A_Y6” Pin Assignment.

| Flex-Circuit Connector A_Y7 <i>(connects module Y7_TL, Y7_BR, Y7_TR or Y7_BL)</i> | | | | |
|---|--------------|----------------|--------------|----------------|
| | Pin # | Signal | Pin # | Signal |
| | 1 | A_Y7_Vbias(+) | 41 | A_Y7_Vbias(-) |
| | 2 | *REMOVED* | 42 | *NO CONNECT* |
| | 3 | *REMOVED* | 43 | *NO CONNECT* |
| | 4 | *REMOVED* | 44 | *NO CONNECT* |
| | 5 | *REMOVED* | 45 | *NO CONNECT* |
| | 6 | *REMOVED* | 46 | A_Y7_INJECT(+) |
| | 7 | *REMOVED* | 47 | A_Y7_INJECT(-) |
| | 8 | A_Y7_DGND | 48 | A_Y7_AGND |
| | 9 | A_Y7_Vddd | 49 | A_Y7_Vdda |
| | 10 | A_Y7_Vddd | 50 | A_Y7_Vdda |
| | 11 | A_Y7_Vddd | 51 | A_Y7_Vdda |
| | 12 | A_Y7_DSense(+) | 52 | A_Y7_ASense(+) |
| | 13 | A_Y7_DSense(-) | 53 | A_Y7_ASense(-) |
| | 14 | A_Y7_DGND | 54 | A_Y7_AGND |
| | 15 | A_Y7_DGND | 55 | A_Y7_AGND |
| | 16 | A_Y7_DGND | 56 | A_Y7_AGND |
| | 17 | A_Y7_GPIO1(+) | 57 | A_Y7_GPIO13(+) |
| | 18 | A_Y7_GPIO1(-) | 58 | A_Y7_GPIO13(-) |
| | 19 | A_Y7_GPIO2(+) | 59 | A_Y7_GPIO14(+) |
| | 20 | A_Y7_GPIO2(-) | 60 | A_Y7_GPIO14(-) |
| | 21 | A_Y7_GPIO3(+) | 61 | A_Y7_GPIO15(+) |
| | 22 | A_Y7_GPIO3(-) | 62 | A_Y7_GPIO15(-) |
| | 23 | A_Y7_GPIO4(+) | 63 | A_Y7_GPIO16(+) |
| | 24 | A_Y7_GPIO4(-) | 64 | A_Y7_GPIO16(-) |
| | 25 | A_Y7_GPIO5(+) | 65 | A_Y7_GPIO17(+) |
| | 26 | A_Y7_GPIO5(-) | 66 | A_Y7_GPIO17(-) |
| | 27 | A_Y7_GPIO6(+) | 67 | A_Y7_GPIO18(+) |
| | 28 | A_Y7_GPIO6(-) | 68 | A_Y7_GPIO18(-) |
| | 29 | A_Y7_GPIO7(+) | 69 | A_Y7_GPIO19(+) |
| | 30 | A_Y7_GPIO7(-) | 70 | A_Y7_GPIO19(-) |
| | 31 | A_Y7_GPIO8(+) | 71 | A_Y7_GPIO20(+) |
| | 32 | A_Y7_GPIO8(-) | 72 | A_Y7_GPIO20(-) |
| | 33 | A_Y7_GPIO9(+) | 73 | A_Y7_GPIO21(+) |
| | 34 | A_Y7_GPIO9(-) | 74 | A_Y7_GPIO21(-) |
| | 35 | A_Y7_GPIO10(+) | 75 | A_Y7_GPIO22(+) |
| | 36 | A_Y7_GPIO10(-) | 76 | A_Y7_GPIO22(-) |
| | 37 | A_Y7_GPIO11(+) | 77 | A_Y7_GPIO23(+) |
| | 38 | A_Y7_GPIO11(-) | 78 | A_Y7_GPIO23(-) |
| | 39 | A_Y7_GPIO12(+) | 79 | A_Y7_GPIO24(+) |
| | 40 | A_Y7_GPIO12(-) | 80 | A_Y7_GPIO24(-) |

Table 46. Flex-Circuit Connector “A_Y7” Pin Assignment.

| Flex-Circuit Connector A_Y8 <i>(connects module Y8_TR or Y8_BL)</i> | | | | |
|---|--------------|----------------|--------------|----------------|
| | Pin # | Signal | Pin # | Signal |
| | 1 | A_X4_GPIO12(-) | 41 | A_X4_GPIO24(-) |
| | 2 | A_X4_GPIO12(+) | 42 | A_X4_GPIO24(+) |
| | 3 | A_X4_GPIO11(-) | 43 | A_X4_GPIO23(-) |
| | 4 | A_X4_GPIO11(+) | 44 | A_X4_GPIO23(+) |
| | 5 | A_X4_GPIO10(-) | 45 | A_X4_GPIO22(-) |
| | 6 | A_X4_GPIO10(+) | 46 | A_X4_GPIO22(+) |
| | 7 | A_X4_GPIO9(-) | 47 | A_X4_GPIO21(-) |
| | 8 | A_X4_GPIO9(+) | 48 | A_X4_GPIO21(+) |
| | 9 | A_X4_GPIO8(-) | 49 | A_X4_GPIO20(-) |
| | 10 | A_X4_GPIO8(+) | 50 | A_X4_GPIO20(+) |
| | 11 | A_X4_GPIO7(-) | 51 | A_X4_GPIO19(-) |
| | 12 | A_X4_GPIO7(+) | 52 | A_X4_GPIO19(+) |
| | 13 | A_X4_GPIO6(-) | 53 | A_X4_GPIO18(-) |
| | 14 | A_X4_GPIO6(+) | 54 | A_X4_GPIO18(+) |
| | 15 | A_X4_GPIO5(-) | 55 | A_X4_GPIO17(-) |
| | 16 | A_X4_GPIO5(+) | 56 | A_X4_GPIO17(+) |
| | 17 | A_X4_GPIO4(-) | 57 | A_X4_GPIO16(-) |
| | 18 | A_X4_GPIO4(+) | 58 | A_X4_GPIO16(+) |
| | 19 | A_X4_GPIO3(-) | 59 | A_X4_GPIO15(-) |
| | 20 | A_X4_GPIO3(+) | 60 | A_X4_GPIO15(+) |
| | 21 | A_X4_GPIO2(-) | 61 | A_X4_GPIO14(-) |
| | 22 | A_X4_GPIO2(+) | 62 | A_X4_GPIO14(+) |
| | 23 | A_X4_GPIO1(-) | 63 | A_X4_GPIO13(-) |
| | 24 | A_X4_GPIO1(+) | 64 | A_X4_GPIO13(+) |
| | 25 | A_X4_DGND | 65 | A_X4_AGND |
| | 26 | A_X4_DGND | 66 | A_X4_AGND |
| | 27 | A_X4_DGND | 67 | A_X4_AGND |
| | 28 | A_X4_DSense(-) | 68 | A_X4_ASense(-) |
| | 29 | A_X4_DSense(+) | 69 | A_X4_ASense(+) |
| | 30 | A_X4_Vddd | 70 | A_X4_Vdda |
| | 31 | A_X4_Vddd | 71 | A_X4_Vdda |
| | 32 | A_X4_Vddd | 72 | A_X4_Vdda |
| | 33 | A_X4_DGND | 73 | A_X4_AGND |
| | 34 | *REMOVED* | 74 | A_X4_INJECT(-) |
| | 35 | *REMOVED* | 75 | A_X4_INJECT(+) |
| | 36 | *REMOVED* | 76 | *NO CONNECT* |
| | 37 | *REMOVED* | 77 | *NO CONNECT* |
| | 38 | *REMOVED* | 78 | *NO CONNECT* |
| | 39 | *REMOVED* | 79 | *NO CONNECT* |
| | 40 | A_X4_Vbias(+) | 80 | A_X4_Vbias(-) |

Table 47. Flex-Circuit Connector “A_Y8” Pin Assignment.

| Flex-Circuit Connector A_Y9 <i>(connects module Y9_TR or Y9_BL)</i> | | | | |
|---|--------------|------------------|--------------|------------------|
| | Pin # | Signal | Pin # | Signal |
| | 1 | A_X7Y9_Vbias(+) | 41 | A_X7Y9_Vbias(-) |
| | 2 | *REMOVED* | 42 | *NO CONNECT* |
| | 3 | *REMOVED* | 43 | *NO CONNECT* |
| | 4 | *REMOVED* | 44 | *NO CONNECT* |
| | 5 | *REMOVED* | 45 | *NO CONNECT* |
| | 6 | *REMOVED* | 46 | A_X7Y9_INJECT(+) |
| | 7 | *REMOVED* | 47 | A_X7Y9_INJECT(-) |
| | 8 | A_X7Y9_DGND | 48 | A_X7Y9_AGND |
| | 9 | A_X7Y9_Vddd | 49 | A_X7Y9_Vdda |
| | 10 | A_X7Y9_Vddd | 50 | A_X7Y9_Vdda |
| | 11 | A_X7Y9_Vddd | 51 | A_X7Y9_Vdda |
| | 12 | A_X7Y9_DSense(+) | 52 | A_X7Y9_ASense(+) |
| | 13 | A_X7Y9_DSense(-) | 53 | A_X7Y9_ASense(-) |
| | 14 | A_X7Y9_DGND | 54 | A_X7Y9_AGND |
| | 15 | A_X7Y9_DGND | 55 | A_X7Y9_AGND |
| | 16 | A_X7Y9_DGND | 56 | A_X7Y9_AGND |
| | 17 | A_X7Y9_GPIO1(+) | 57 | A_X7Y9_GPIO13(+) |
| | 18 | A_X7Y9_GPIO1(-) | 58 | A_X7Y9_GPIO13(-) |
| | 19 | A_X7Y9_GPIO2(+) | 59 | A_X7Y9_GPIO14(+) |
| | 20 | A_X7Y9_GPIO2(-) | 60 | A_X7Y9_GPIO14(-) |
| | 21 | A_X7Y9_GPIO3(+) | 61 | A_X7Y9_GPIO15(+) |
| | 22 | A_X7Y9_GPIO3(-) | 62 | A_X7Y9_GPIO15(-) |
| | 23 | A_X7Y9_GPIO4(+) | 63 | A_X7Y9_GPIO16(+) |
| | 24 | A_X7Y9_GPIO4(-) | 64 | A_X7Y9_GPIO16(-) |
| | 25 | A_X7Y9_GPIO5(+) | 65 | A_X7Y9_GPIO17(+) |
| | 26 | A_X7Y9_GPIO5(-) | 66 | A_X7Y9_GPIO17(-) |
| | 27 | A_X7Y9_GPIO6(+) | 67 | A_X7Y9_GPIO18(+) |
| | 28 | A_X7Y9_GPIO6(-) | 68 | A_X7Y9_GPIO18(-) |
| | 29 | A_X7Y9_GPIO7(+) | 69 | A_X7Y9_GPIO19(+) |
| | 30 | A_X7Y9_GPIO7(-) | 70 | A_X7Y9_GPIO19(-) |
| | 31 | A_X7Y9_GPIO8(+) | 71 | A_X7Y9_GPIO20(+) |
| | 32 | A_X7Y9_GPIO8(-) | 72 | A_X7Y9_GPIO20(-) |
| | 33 | A_X7Y9_GPIO9(+) | 73 | A_X7Y9_GPIO21(+) |
| | 34 | A_X7Y9_GPIO9(-) | 74 | A_X7Y9_GPIO21(-) |
| | 35 | A_X7Y9_GPIO10(+) | 75 | A_X7Y9_GPIO22(+) |
| | 36 | A_X7Y9_GPIO10(-) | 76 | A_X7Y9_GPIO22(-) |
| | 37 | A_X7Y9_GPIO11(+) | 77 | A_X7Y9_GPIO23(+) |
| | 38 | A_X7Y9_GPIO11(-) | 78 | A_X7Y9_GPIO23(-) |
| | 39 | A_X7Y9_GPIO12(+) | 79 | A_X7Y9_GPIO24(+) |
| | 40 | A_X7Y9_GPIO12(-) | 80 | A_X7Y9_GPIO24(-) |

Table 48. Flex-Circuit Connector “A_Y9” Pin Assignment.

5 FTB POWER CONSUMPTION

FPIX 2

| Current | Typical | Maximum |
|---------|---------|---------|
| Ia@2.5V | 60mA | 80mA |
| Id@2.5V | 80mA | 100mA |
| Power | | |
| Pa | 0.15W | 0.20W |
| Pd | 0.20W | 0.25W |

MODULE

| Current(4x1) | Typical | Maximum | Power (typical) |
|--------------|---------|---------|--------------------|
| Ia@2.5V | 240mA | 320mA | 0.60W |
| Id@2.5V | 320mA | 400mA | 0.80W |
| Current(5x1) | | | |
| Ia@2.5V | 300mA | 400mA | 0.75W |
| Id@2.5V | 400mA | 500mA | 1.00W |
| Current(6x1) | | | |
| Ia@2.5V | 360mA | 480mA | 0.90W |
| Id@2.5V | 480mA | 600mA | 1.20W |

5.1 POWER CONSUMPTION PER STATION

1 Station = 24 modules (4x1) +18 modules (5x1) +14 modules (6x1)

CURRENT

| 24 modules (4x1) | Typical | Maximum |
|------------------------|---------|---------|
| Ia@2.5V | 5.760A | 7.680A |
| Id@2.5V | 7.680A | 9.600A |
| 18 modules (5x1) | | |
| Ia@2.5V | 5.400A | 7.200A |
| Id@2.5V | 7.200A | 9.000A |
| 14 modules (6x1) | | |
| Ia@2.5V | 5.040A | 6.720A |
| Id@2.5V | 6.720A | 8.400A |
| Total Ia per station | 16.200A | 21.600A |
| Total Id per station | 21.600A | 27.000A |
| Total Ia (30 stations) | 486.0A | 648.0A |
| Total Id (30 stations) | 648.0A | 810.0A |
| Total Id+Ia | 1134.0A | 1458.0A |

POWER

| | | |
|------------------------|---------|---------|
| Total Pa per station | 40.5W | 54.0W |
| Total Pd per station | 54.0W | 67.5W |
| Total Pa (30 stations) | 1215.0W | 1620.0W |
| Total Pd (30 stations) | 1620.0W | 2025.0W |
| Total Pd+Pa | 2835.0W | 3645.0W |

5.2 TYPICAL AVERAGE CURRENT CONSUMPTION PER CONNECTOR

1/4 Station BR = 70 FPIX2 (14 modules)-

•(1) Analog Connector [(4.2A)/14 conductors] = 300mA/wire

•(1) Digital Connector [(5.6A)/14 conductors] = 400mA/wire

1/4 Station BL = 65 FPIX2 (14 modules)-

•(1) Analog Connector [(3.9A)/14 conductors] = 279mA/wire

•(1) Digital Connector [(5.2A)/14 conductors] = 372mA/wire

1/4 Station TR = 65 FPIX2 (14 modules)-

•(1) Analog Connector [(3.9A)/14 conductors] = 279mA/wire

•(1) Digital Connector [(5.2A)/14 conductors] = 372mA/wire

1/4 Station TL = 70 FPIX2 (14 modules)-

•(1) Analog Connector [(4.2A)/14 conductors] = 300mA/wire

(1) Digital Connector [(5.6A)/14 conductors] = 400mA/wire

5.3 ANALOG AND DIGITAL POWER CONSUMPTION

| 24 modules (4x1) | Current | Power |
|------------------------|---------|---------|
| Ia@2.77V | 5.760A | 15.95W |
| 18 modules (5x1) | | |
| Ia@2.83V | 5.400A | 15.30W |
| 14 modules (6x1) | | |
| Ia@2.90V | 5.040A | 14.62W |
| Total Ia per station | 16.200A | 45.87W |
| Total Ia (30 stations) | 486.0A | 1316.1W |

* POWER LOSS CONSIDERED USING 22AWG CABLES

Power consumption at HDI=1215.0W

Power loss in the wires = 101 W

Power consumption at power supply= 1316.1W

| 24 modules (4x1) | Current | Power |
|------------------------|---------|--------|
| Id@2.83V | 7.68A | 21.74W |
| 18 modules (5x1) | | |
| Id@2.94V | 7.20A | 21.17W |
| 14 modules (6x1) | | |
| Id@3.03V | 6.72A | 20.36W |
| Total Ia per station | 21.60A | 63.30W |
| Total Ia (30 stations) | 648A | 1900W |

* POWER LOSS CONSIDERED USING 22AWG CABLES

Power consumption at HDI= 1620W

Power loss in the wires = 280 W

Power consumption at power supply= 1900W

Using a AWG 26 solid copper conductor:

1.43 ohms – 10m

2.86 ohms – 20m (WIx+WIx gnd)

Ia (4x1)= 240mA Vdrop=0.68V @20m

Ia (5x1)= 300mA Vdrop=0.85V @20m

Ia (6x1)= 360mA Vdrop=1.03V @20m

Id (4x1)= 320mA Vdrop=0.92V @20m

Id (5x1)= 400mA Vdrop=1.15V @20m

Id (6x1)= 480mA Vdrop=1.38V @20m

Using a AWG 24 solid copper conductor:

0.90 ohms – 10m

1.80 ohms – 20m (WIx+WIx gnd)

Ia (4x1)= 240mA Vdrop=0.44V @20m

Ia (5x1)= 300mA Vdrop=0.54V @20m

Ia (6x1)= 360mA Vdrop=0.65V @20m

Id (4x1)= 320mA Vdrop=0.58V @20m

Id (5x1)= 400mA Vdrop=0.72V @20m

Id (6x1)= 480mA Vdrop=0.87V @20m

Using a AWG 22 solid copper conductor:

0.55 ohms – 10m (WIx)

1.10 ohms – 20m (WIx+WIx gnd)

Ia (4x1)= 240mA Vdrop=0.27V @20m

Ia (5x1)= 300mA Vdrop=0.33V @20m

Ia (6x1)= 360mA Vdrop=0.40V @20m

Id (4x1)= 320mA Vdrop=0.36V @20m

Id (5x1)= 400mA Vdrop=0.44V @20m

Id (6x1)= 480mA Vdrop=0.53V @20m

Using a AWG 20 solid copper conductor:

0.34 ohms – 10m

0.68 ohms – 20m (WIx+WIx gnd)

Ia (4x1)= 240mA Vdrop=0.17V @20m

Ia (5x1)= 300mA Vdrop=0.20V @20m

Ia (6x1)= 360mA Vdrop=0.25V @20m

Id (4x1)= 320mA Vdrop=0.22V @20m

Id (5x1)= 400mA Vdrop=0.28V @20m

Id (6x1)= 480mA Vdrop=0.33V @20m